

# A GALS APPROACH TO IMPROVE SYSTEM INTEGRATION

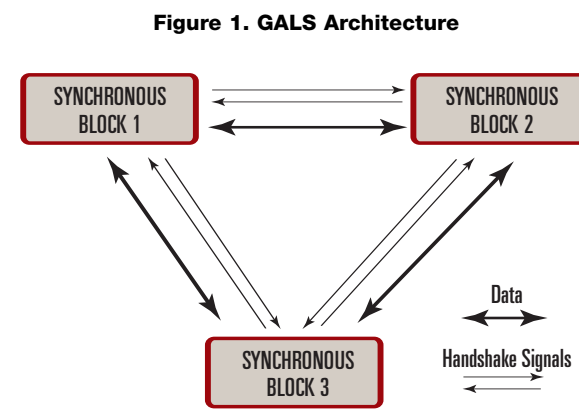
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System-on-chip (SOC) integration imposes a number of technical challenges on designers and tools. The increased complexity, performance requirements and the need to reduce power consumption and electromagnetic interference (EMI) must be efficiently addressed. Furthermore, the continued technology improvement towards nanoscale dimensions generates additional challenges.

Many of these challenges are associated with the design of a clock network in digital systems. Clock skew is a severe bottleneck for complex digital circuits. The synchronous transitions of clock signals are a strong source of noise and EMI. Additionally, the power spent to run only a clock tree is comparable to the power consumed in the functional blocks of a system. Splitting a complex digital system into several independent subsystems will reduce problems significantly. Dealing with smaller blocks is much simpler, and power saving techniques can be more successfully applied. Crosstalk and EMI are suppressed due to the uncorrelated operation of autonomous blocks. However, synchronization between blocks operating at different speeds and clock frequencies does become more complicated.

Several approaches address the problem of block partitioning and data synchronization between independent blocks, while some explicitly focus on power consumption and EMI. Today, these techniques are primarily referred to as globally asynchronous locally synchronous (GALS) methods. Many of these techniques are not generally applicable; however, some of them are currently used in design practice.

All GALS systems have a common general structure. A basic GALS paradigm is based on a system composed of a number of synchronous modules designed in a traditional way. However, it is assumed that clocks of such synchronous modules are not necessarily correlated, and consequently, the synchronous modules communicate asynchronously using handshake channels. For this purpose, locally synchronous modules are usually surrounded by asynchronous wrappers facilitating such inter-module data transfer. The principle architecture of GALS systems for point-to-point dataflow structures is illustrated in Figure 1. For inter-block communication, practical GALS implementations may form more complex structures, such as bus or network-on-chip (NoC) structures. Even though different data synchronization mechanisms can be used, all GALS proposals are based on the simple structure shown in Figure 1.



There are three major techniques used to safely transfer data between locally synchronous blocks and to avoid metastability in GALS systems: pausable local clocks, boundary or interface synchronization, and first in, first out (FIFO)-like communication structures<sup>1</sup>.

## POWER SAVING WITH GALS

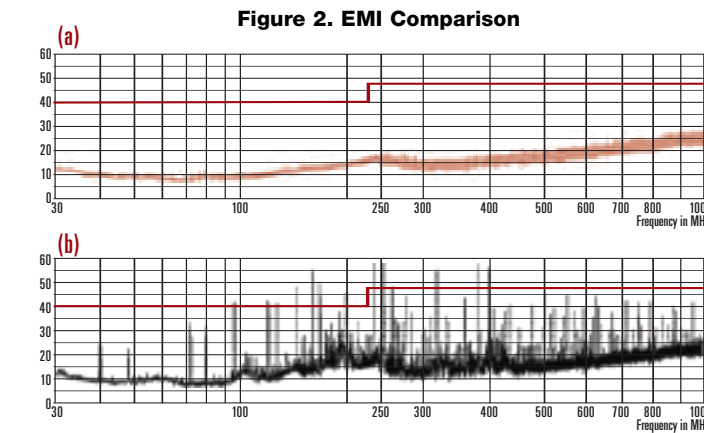
The inherent power reduction obtained by using a GALS-based system is essentially based on the same paradigm as the low-power techniques used for synchronous circuits – trigger the locally synchronous block only when needed, and lower to a minimum the switching activity.

Even more power savings can be expected if the GALS approach is applied together with voltage and frequency scaling. The GALS architecture is very well suited for such a technique since the communication between blocks is asynchronous. The boundaries of GALS blocks are clearly defined, and partitioning naturally leads to a hierarchical layout process. Therefore, the introduction of different power rings in layout and the insertion of direct current-to-direct current (DC-DC) converters become easier. Theoretical investigations presented by Emil Talpes and Diana Marculescu<sup>2</sup> show that an average energy reduction of up to 33 percent can be obtained at a performance degradation of about 10 percent.

## EMI REDUCTION WITH GALS

Another very important benefit of GALS designs is the reduction of EMI. It has been demonstrated that asynchronous circuits expose significantly lower levels of EMI than their synchronous counterparts. One example is shown in Figure 2 which compares the asynchronous

Amulet 2 processor with a synchronous ARM9<sup>3</sup>. Lowering the noise generated by the digital part of the system is an important SOC integration issue. Other studies suggest the possibility of reducing the noise spectrum on a power supply line by up to 20dB in comparison with a synchronous design. Additionally, a 40 percent reduction in supply current peaks can be expected<sup>1</sup>.



(a) Amulet 2; (b) compatible synchronous ARM9 processor

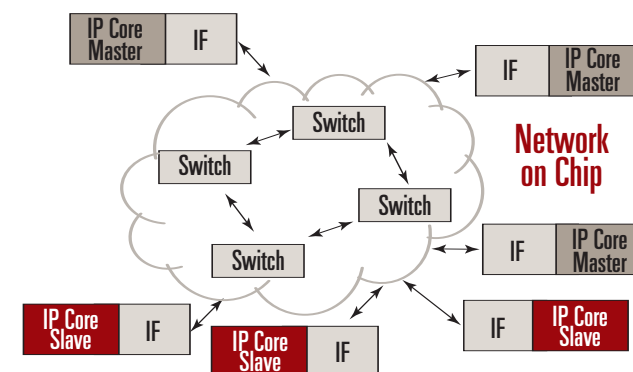
This benefit can also be very useful for security applications. GALS circuits have the potential to increase immunity toward differential power analysis (DPA) attacks<sup>4</sup>. The power spectrum of an asynchronous circuit does not contain large peaks at the global clock frequency and at its harmonics, and therefore is expected to supply potential attackers with less information about the circuit operation. Furthermore, due to their asynchronous components, GALS chips are less controllable, and their timing is less deterministic.

## STATE-OF-THE-ART GALS DESIGN AND NOCS

Although transistor performance will continue to improve, the performance of interconnection networks cannot keep up with this progress. Employing self-timed techniques for interconnect networks is a promising means to tackle a number of on-chip interconnection issues, from power and EMI reduction to clock skew management and modularity of design. A promising target platform can be seen in the area of NoCs. The NoC paradigm seems to be a very attractive generalized solution for future chip interconnect. A typical NoC architecture is illustrated in Figure 3.

The CHAIN network developed by Bainbridge<sup>5</sup> is interesting in that it is entirely implemented using asynchronous, or clockless, circuit techniques. CHAIN is targeted to heterogeneous low-power

Figure 3. Typical NoC Architecture



systems, in which the network is system-specific. It has been implemented in a smart card which benefits from the low idle power of asynchronous circuits.

There are a few other noteworthy GALS NoC approaches, including Nexus, an asynchronous on-chip network developed at Fulcrum Microsystems<sup>6</sup>; the MANGO network, a NoC targeted to coarse-grained, GALS-type SOCs developed at TU Denmark<sup>7</sup>; and Asynchronous NoC (ANOC), a NoC proposed by LETI<sup>8</sup> which provides low-latency services.

The main reasons for the application of GALS in NoC systems include:

- Global clock skew problems are avoided.
- High potential for power savings (50 percent of a NoC's power is consumed by the clock net, which the GALS approach could significantly reduce).
- The synchronous parts of NoC nodes are designed at their optimum clock frequency.
- GALS facilitates process variation-tolerant, on-chip interconnection schemes.
- GALS inherently generates low EMI.

While progress in clocking structures within NoCs continues (e.g., advanced back-end synthesis tools and aggressive clock gating), it is quite clear that a complete paradigm shift towards GALS would enable significant advantages for real chip realizations.

## FUTURE CHALLENGES FOR THE GALS PARADIGM

Although GALS systems are popular in the scientific community, they are not frequently used in commercial systems. By partitioning a complex synchronous system into a number of independent subsystems, a company can immediately benefit from reduced clock skew, a simpler clock tree and easier timing closure. Eventually, this may also result in a shorter design process and improved time-to-market. However, there are still challenges that must be resolved before the GALS design is established as a mainstream design technique.

One issue that has slowed the practical adoption of the GALS methodology is the lack of mature design flows. The classical synchronous design methodology is well supported by a number of established computer-aided design (CAD) tools which are constantly being improved. But they do not efficiently support asynchronous design (except for a few tools from smaller start-up companies). Consequently, the asynchronous design community must use tools developed in academia. However, such tools are usually uncoordinated, incomplete and improvement is erratic. Therefore, many steps in the design process for asynchronous circuits are still manual, and there is no consistent design flow from behavioral modeling to tape-out of the circuit.

A similar problem exists with test flows. A usual test flow for synchronous circuits is based on the application of well-known scan chains that can be used to control and observe all sequential elements within a design. The scan chain approach requires a centralized clock, which is not available and not reasonable in standard asynchronous circuits. But there are some solutions that offer a similar structural test approach for asynchronous circuits<sup>9</sup>. In addition, the test strategy for GALS systems usually includes the functional testing of the asynchronous control part of the system

## Tools Aid in IP Risk Assessment Process

GSA is pleased to offer a new suite of productivity tools that enables more efficient communication between IP vendors, IP integrators and foundries for IP integration, an area critical for design success. The tools create efficiencies and lower risk by reducing the time spent collecting the specific information required to purchase, integrate and utilize IP.

### GSA Hard IP Quality Risk Assessment Tool Available for Download

The first tool in the suite, addressing hard IP quality, is available complimentary to the industry. It enables companies to collect important information about an IP vendor, its design methodology and the IP under evaluation to enable risk assessment across seven categories: IP design, integration, verification, process technology, product documentation, reliability and test.

### GSA Hard IP Licensing Risk Assessment Tool

The second tool in the suite, the Licensing Tool, focuses on assessing the licensing risk an integrator is willing to accept before acquiring the desired IP. Designed for semiconductor companies, the Licensing Tool provides a benchmark set of questions that cover the major areas of IP licensing and acquisition, including scope of license, payment, warranty, limitation of liability, indemnity, governing law, confidentiality and term and termination.

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#### Member Benefits *continued from page 39*

- Reduce time from product specification to delivery.
- Bring CE manufacturers new product ideas sooner.
- Work more closely to reduce product costs.

While they agree in principal, they disagree as to the priority. Both agree that reducing time from product specification to delivery is the number-one priority; however, they differ on priorities two and three. Based on the survey results, nearly a quarter of IC respondents feel that the second priority should be to work more closely with CE manufacturers to reduce product costs. CE respondents ranked this priority third. CE respondents feel that the second priority should be that IC suppliers bring new product/feature ideas to CE manufacturers sooner. But IC suppliers feel that for them to bring new product/feature ideas sooner, they need to be involved in the design process earlier.

#### CE Companies Want Earlier IC Supplier Involvement

To get products to market faster, CE manufacturers and IC suppliers must create a more collaborative environment. They need to communicate throughout the design and production phases. According to the survey results, CE and IC respondents differ in how they collaborate and what their priorities are during the production process. For example, CE producers believe that IC suppliers should become involved during the concept or definition phases and expect the highest support at the design-start and cost-reduction phases. The results also indicate that IC suppliers are more likely to get involved during the definition phase. This leads to the CE manufacturer having more control over the process and design of the product.

#### Non-Standardized CE Design Methodology is a Major IC Challenge

CE and IC respondents differed greatly on design standardization. Most IC suppliers generally have a standardized methodology and screen

rigorously at the design concept phase regarding design starts, while CE respondents affirmed that they don't have a stated methodology, or that it varies and evolves over time. Creating commonality of definition and agreement on product design will go a long way toward improving cost, time-to-market and product quality.

### GSA AND CEA COLLABORATE ON NEW INITIATIVES FOR 2009

This report has provided GSA, CEA and KPMG with a strong platform for facing the challenges that CE companies and IC suppliers must deal with. To provide a more in-depth study of the issues plaguing CE manufacturers and IC suppliers, GSA and CEA will continue to collaborate on new research initiatives to support the CE and semiconductor industries on solving some of the time-to-market, profit and time-to-revenue issues they currently face. For example, one avenue available to IC suppliers is to work with consumers to identify system needs earlier, which would shorten their design cycles and improve their time-to-market challenges. By learning what market trends are evolving, IC suppliers can begin the process of reducing the production cycle and ramping up output for their CE counterparts.

GSA and CEA will conduct a follow-up survey that will dig deeper into the findings identified by "the CE boom." To provide more value to the consumer and semiconductor supply chains, both organizations understand that the success of these two industries relies on improved collaborative efforts between CE manufacturers and IC suppliers. As part of that recognition, GSA and CEA are committed to facilitating research that will identify potential solutions that will enable both industries to meet their fiscal and production goals. ■

#### GALS *continued from page 13*

and a built-in self-test (BIST) approach.

Finally, many digital designers have only limited experience with asynchronous design. But asynchronous and GALS designs have their own properties and design constraints which are sometimes not easily adopted by synchronous designers. Small but non-standard modifications of locally synchronous blocks are often required to implement a safe and reliable asynchronous operation.

To cope with these issues, there are several research initiatives driven from academia and industry. One such initiative is GALS Interface for Complex Digital System Integration (GALAXY)<sup>10</sup>, which is funded by the EU to address the design flows and methodologies of future GALS systems.

#### CONCLUSION

GALS design is a promising option to improve SOC design and integration, and as a back-end, physical-level infrastructure for NoCs. Additional benefits are created in the areas of low-power design, low EMI and the ability to cope with higher variability in nanoscale systems.

The GALS methodology cannot yet develop its full potential due to low CAD support in terms of design and test flow. However, these issues are now addressed by various research initiatives such as GALAXY.

The further miniaturization of semiconductor devices and the migration to 28-nanometer CMOS technologies and below will most likely lead to more frequent application of the GALS methodology and systems. ■

#### About the Authors

Milos Krstic received a Dr. Ing. degree in electronics from Brandenburg University of Technology, Cottbus, Germany in 2006. Since 2001, he has been with IHP Microelectronics, Frankfurt (Oder), Germany. For the last few years, his work was mainly focused on low-power digital design for wireless applications and GALS methodologies for digital systems integration. He is currently a coordinator of the EU-funded GALAXY project on GALS design ([www.galaxy-project.org](http://www.galaxy-project.org)). You can reach Milos Krstic at [krstic@ihp-microelectronics.com](mailto:krstic@ihp-microelectronics.com).

Eckhard Grass received a Dr. Ing. degree in electronics from the Humboldt University of Berlin, Germany in 1993. Since 1999, he has been with IHP GmbH, Frankfurt (Oder), Germany leading a number of projects on the implementation of wireless broadband communication systems in the 5GHz and

#### Partnership *continued from page 23*

applications such as audio codecs. Specialty foundries target IP providers that service their customers' specific needs and will increase the level of sophistication they offer in the products they manufacture. As technology development costs continue to rise, it is expected that the benefit from and trend of partnering with IP providers will increase and further strengthen the position of specialty foundries that leverage these strategic relationships.

#### CONCLUSION

It is expected that foundries will account for almost 40 percent of total semiconductor revenue by 2012, whereas today they account for 25 percent. Specialty foundries will help drive this growth and will do so in a business model that is viable, offering potential for higher economic returns for foundry players, as well as benefiting fabless and IDM players with the increased availability of advanced, customized technologies. ■

60GHz bands. Eckhard has registered four patents and published a number of papers mainly in the areas of circuits for wireless communications and asynchronous circuit design. You can reach Eckhard Grass at [grass@ihp-microelectronics.com](mailto:grass@ihp-microelectronics.com).

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#### Resources

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- <sup>10</sup> [www.galaxy-project.org](http://www.galaxy-project.org).

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