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Report containing summary of all publications, presentations, and patent applications generated within the project

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This is a reporting including the complete list of the published/accepted publications up to the project end.

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GALAXY

GALS InterfAce for CompleX Digital
SYstem Integration

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1 SUMMARY OF THE PUBLICATIONS

In the following list we are summarizing all publications from GALAXY project:

1.1 JOURNAL AND CONFERENCE PUBLICATIONS

1. M. Krstic, M.Piz, M. Ehrig, E. Grass, [OFDM Datapath Baseband Processor for 1 Gbps Datarate](#), Proc. IFIP/IEEE VLSI-SoC Conference, Rhodes Island, Greece, October 2008, pp. 156-159.
2. Alberto Ferrante, Simone Medardoni, Davide Bertozzi, [Network Interface Sharing Techniques for Area Optimized NoC Architectures](#), 11th EUROMICRO Conference on Digital System Design Architectures, Methods and Tools, DSD 2008, September 3-5, 2008, Parma, Italy.
3. G.Paci, A. Nackaerts, F.Catthoor, L.Benini, P.Marchal, [How to Live with Uncertainties: Exploiting the Performance Benefits of Self-Timed Logic In Synchronous Design](#), 11th EUROMICRO Conference on Digital System Design Architectures, Methods and Tools, DSD 2008, September 3-5, 2008, Parma, Italy.
4. D.Ludovici, S.Medardoni, F.Gilabert, D.Bertozzi, G.Gaydadjev, C.Gomez, M.E.Gomez, P.Lopez, Assessing Fat-Tree Topologies for Regular Network-on-Chip Design under Nanoscale Technology Constraints, DATE 2009.
5. G.Paci, D.Bertozzi, L.Benini, Effectiveness of Adaptive Supply Voltage and Body Bias as Post-Silicon Variability Compensation Techniques for Full-Swing and Low-Swing On-Chip Communication Channels, DATE 2009.
6. Bertozzi, Benini, Gilabert, Ludovici, Gaydadjev, Designing Regular Network-on-Chip Topologies under Technology, Architecture and Software Constraints, International Workshop on Multi-Core Computing Systems (MuCoCos09), Japan, March 2009.
7. M. Krstic, X. Fan, E. Grass, F. Gürkaynak, GALS for Bursty Data Transfer based on Clock Coupling, In Proc. Fourth International Workshop on Formal Methods for Globally Asynchronous Locally Synchronous Design (FMGALS'09), A DATE'09 Friday Workshop, April 24., Nice, France, ENTCS 17588, Vol 245, pp. 103-113,.
8. T. Krol, M. Krstic, X. Fan, E. Grass, Modeling and Reducing EMI in GALS and Synchronous Systems, In Proc. International Workshop on Power And Timing Modeling, Optimization and Simulation (PATMOS) 2009.
9. D. Ludovici, A. Strano, D. Bertozzi, G. Gaydadjev, L. Benini, Comparing Tightly and Loosely Coupled Mesochronous Synchronizers in a NoC Switch Architecture, Proceedings of NoCs 2009.
10. S.Rodrigo, S.Medardoni, J.Flich, D.Bertozzi, J.Duato, Efficient Implementation of Distributed Routing Algorithms for NoCs, IET-CDT Journal, special issue on NoCs, Vol.3 No. 5, pp. 157, 2009.
11. T.Skeie, F.O.S.Jacobsen, S.Rodrigo, J.Flich, S.Medardoni, D.Bertozzi, Flexible DOR Routing for Virtualization of Multicore Chips, International Symposium on System-on-Chip, Tampere, 2009.



12. X. Fan, M. Krstic, E. Grass, [Analysis and Optimization of Pausible Clocking based GALS Design](#), In Proc. XXVII IEEE International Conference on Computer Design (ICCD) 2009, Resort at Squaw Creek, Lake Tahoe, California, pp. 358-365, "Best Paper" Award.
13. A.Strano, D.Ludovici, D.Bertozzi, "Architecture Design Principles for the Integration of Synchronization Interfaces into Network-on-Chip Switches", Proc. of NoCArC2009, New York, pp. 31-36.
14. D.Ludovici, A.Strano, D.Bertozzi, L.Benini, G.Gaydadjiev, "Design Space Exploration of a Cost-Effective and Flexible Mesochronous NoC Architecture for GALS Systems", DATE2010
15. Lilian Janin, Shoujie Li and Doug Edwards, Integrated Design Environment for Reconfigurable HPC, ARC 2010, the 6th International Symposium on Applied Reconfigurable Computing, Springer Verlag LNCS series volume (Lecture Notes in Computer Science).
16. M. Krstic, T. Krol, X. Fan, E. Grass, Reducing EMI using GALS Approach, Journal of Low Power Electronics (JOLPE), Volume 6, Number 1, April 2010, pp. 181-191.
17. M. Stanisavljevic, A. Schmid, Y. Leblebici, Selective Redundancy-Based Design Techniques for the Minimization of Local Delay Variations, ISCAS 2010, Paris 2010.
18. X. Fan, M. Krstic, C. Wolf, E. Grass, A GALS FFT Processor with Clock Modulation for Low-EMI Applications, ASAP 2010 - 21st IEEE International Conference on Application-specific Systems, Architectures and Processors, July 7-9, 2010 Rennes, France
19. A.Strano, D.Ludovici, D.Bertozzi, "A Library of Dual-Clock FIFOs for Cost-Effective and Flexible MPSoC Design", SAMOS 2010
20. A.Strano, C.Hernandez, F.Silla, D.Bertozzi, "Process Variation and Layout Mismatch Tolerant Design of Source Synchronous Links for GALS Networks-on-Chip", Symp. on Systems-on-chip 2010.
21. S. Zeidler, A. Bystrov, M. Krstic, R. Kraemer, On-line Testing of Bundled-Data Asynchronous Handshake Protocols, 16th IEEE International On-Line Testing Symposium Corfu Island, Greece, July 5-7, 2010.

1.2 PRESENTATIONS

1. M. Krstic, [Panel: Is networking the solution for interconnect design closure?](#), IP 07 (IP/SoC Conference & Exhibition) (December 5-6, 2007), Grenoble, France, panel membership and presentation.
2. Davide Bertozzi, A silicon-aware design platform for nanoscale networks-on-chip, presented at the Hipeac Interconnect Cluster meeting, during the Hipeac Computing System Week in Paris, November 27th 2008.
3. Daniele Ludovici, "Butterfly vs Unidirectional Fat-Trees for Networks-on-Chip: not a Mere Permutation of Outputs, Presentation of the impact of clock tree on power of regular topologies, Outcome of the Galaxy project, Paphos (Cyprus), Jan 2009, 3rd Workshop on Interconnection Network Architectures: On-Chip, Multi-Chip.
4. Giacomo Paci, Davide Bertozzi, Luca Benini "Effectiveness of adaptive supply voltage and body bias as post-silicon variability compensation techniques for full-swing and low-swing on-chip communication channels", Presentation of the early results of tasks 7.3 of the Galaxy Project, Paphos, Jan 2009, 3rd Workshop on Interconnection Network Architectures: On-Chip, Multi-Chip.



5. Davide Bertozzi, Luca Benini, "Network-on-Chip Technology for Multiprocessor Systems-on-Chip Communication", Presentation of the intermediate outcomes and future goals of the Galaxy Project, Ferrara, Feb 19, 2009, Dissemination of research outcomes to a semiconductor company ST Microelectronics
6. Davide Bertozzi, "Networks-on-Chip: an Implementation Perspective, Presentation of NoC research results. When it came to synchronization issues, presentation of the outcomes of the Galaxy project, Valencia (Spain), June 2009, Occasion: Tutorial given at the DISCA Department of Politechnic University of Valencia
7. Davide Bertozzi, "MPSoC Research at Universities of Bologna and Ferrara, Presentation of the main ongoing research projects at Universities of Bologna and Ferrara, especially the Galaxy Project on leading edge GALS technology, Padua (Italy), Oct 23, 2009, Dissemination of research outcomes to a semiconductor company (Micron Technologies).
8. Daniele Ludovici, Davide Bertozzi, "A GALS Design Methodology for Flexible and Cost-Effective Networks-on-Chip", Presentation of the outcomes of the Galaxy Project (NoC-related issues), Wroclaw (Poland), Oct 27, 2009, Interconnect Cluster Meeting of the Hipecac Network-of-Excellence
9. M. Krstic, GALS Systems with Low-EMI features, Presentation at DAAD Embedded System Workshop, Skopje, Macedonia, Oct 2009
10. D. Ludovici, ["A Complete Design Methodology for GALS Network on Chip"](#), DATE PhD Forum, PhD Forum Poster, Dresden, Mar 2010.
11. M. Krstic, GALS Systems with Low-EMI features, Presentation at DAAD Embedded System Workshop, Nis, Serbia, July 2010
12. M. Krstic, GALS Design for Nanoscale Digital Systems, Presentation at DAAD Embedded System Workshop, Nis, Serbia, July 2010
13. L. Janin, D. Edwards, AsipIDE Tutorial - Bringing together GALS design and open-source tools in a hardware-software-FPGA co-simulation flow, Tutorial at Conference ASYNC-NOCS 2010
14. M. Krstic, E. Grass, X. Fan, S. Zeidler, GALS Workshop for ZUSYS Graduate School, One day tutorial at IHP, Nov 2010.
15. D. Bertozzi, GALAXY Project booth at DATE conference, Apr 2009, Nice, France
16. L. Janin, GALAXY presentation, UNIMAN's 60th Birthday Celebration, June 2008, Manchester, UK.
17. E. Grass, M. Krstic, X. Fan, S. Zeidler, lectures for GALS Workshop in ZUSYS Graduate school, Nov 2010, Frankfurt (Oder), Germany

1.3 BOOKS

1. D.Bertozzi, A.Strano, D.Ludovici, V.Pavlidis, F.Angiolini, M.Krstic,"The Synchronization Challenge", chapter 10 in book "Designing Network-on-Chip Architectures for the Nanoscale Era", edited by José Flich and Davide Bertozzi, CRC Press, 2010
2. X. Fan, M. Krstic, E. Grass, Improvements in Pausible Clocking Scheme for High-Throughput and High-Reliability GALS Systems Design, Springer Monograph on Logic Synthesis 2010, in printing



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1.4 THESIS

1. Tomasz Krol, Globally Asynchronous Locally Synchronous Interfaces Applied for EMI Reduction, Westpomeranian University of Technology, Stetin, Poland

1.5 PATENTS

1. M. Krstić, F. Gürkaynak, X. Fan, E. Grass, GALS circuit block and GALS circuit device suitable for bursty data transfer, submitted to European Patent Office, application number EP08171556.7, date of receipt 12 December 2008, Int. publication date 17.06.2010, International Publication Number WO 2010/066889 A1.
2. X. Fan, M. Krstić, E. Grass, Aussetzbarer Taktgenerator, submitted to Deutsche Patent und Markenamt, application number 800020636, date of receipt 22 Dec 2008, International Publication Date: 1. July 2010, International Publication Number: WO 2010/072548 A1.