



## Deliverable – D12

### *Report on testing and measurements of the first test chip in 130 nm CMOS process provided from IHP*

<b>Grant Agreement No:</b>	214364
<b>Project acronym:</b>	GALAXY
<b>Project title:</b>	GALS InterfAce for CompleX Digital System Integration
<b>Funding Scheme:</b>	STREP
<b>Date of latest version of Annex I against which the assessment will be made:</b>	28.10.2008.
<b>Contractual Date of Delivery to the EC:</b>	31. Jul. 09
<b>Actual Date of Delivery to the EC:</b>	31. Jul. 09
<b>Author(s):</b>	Milos Krstic, Christoph Wolf, Xin Fan (IHP), Milos Stanisavljevic, Stephane Badel, Armin Tajali (EPFL)
<b>Participant(s):</b>	IHP, EPFL
<b>Work Package:</b>	WP7
<b>Security:</b>	Public
<b>Nature:</b>	Report
<b>Version:</b>	1
<b>Total number of pages:</b>	20

#### **Abstract:**

In this report we will provide the results of the testing and measurements of our test chip designed to evaluate the advantages of GALS design. This text consists of two parts: test and measurement setup and strategy and test and measurements results.

**Keyword list: test, EMI, GALS**



# GALAXY

GALS InterfAce for CompleX Digital  
SYstem Integration

Confid. Level: Public  
Date : 31/07/2009  
Issue: 1

<b>Function</b>	<b>Responsibility</b>	<b>Date</b>	<b>Signature</b>
<b>Written by:</b>	Milos Krstic, Christoph Wolf, Xin Fan, Stephane Badel, Armin Tajali, Milos Stanisavljevic	30.7.2009	
<b>Checked by:</b>			
<b>Approved by:</b>			

Reserved to EC

<b>Approved by:</b>			
---------------------	--	--	--



ALMA MATER STUDIORUM  
UNIVERSITA DI BOLOGNA



Never stop thinking



# GALAXY

GALS InterfAce for CompleX Digital  
SYstem Integration

Confid. Level: Public  
Date : 31/07/2009  
Issue: 1

## CHANGE RECORDS

<i>ISSUE</i>	<i>DATE</i>	<i>§ : CHANGE RECORD</i>	<i>AUTHOR</i>
1	30-July-09	First version	Milos Krstic, Christoph Wolf, Xin Fan, Milos Stanisavljevic, Armin Tajali



# GALAXY

GALS InterfACE for CompleX Digital  
SYstem Integration

Confid. Level: Public  
Date : 31/07/2009  
Issue: 1

## BIBLIOGRAPHIC RECORD

Project Number:	214364 GALAXY
Project Title:	GALAXY
Deliverable Type:	Report
Deliverable Number:	D12
Contractual Date of Delivery:	31. Jul. 2009
Actual Date of Delivery:	31. Jul. 2009
Title of Deliverable:	Report on testing and measurements of the first test chip in 130 nm CMOS process provided from IHP
Work package contributing to the Deliverable:	WP7
Authors:	Milos Krstic, Christoph Wolf, Xin Fan, Stephane Badel, Milos Stanisavljevic, Armin Tajali
Abstract	In this report we will provide the results of the testing and measurements of our test chip designed to evaluate the advantages of GALS design. This text consists of two parts: test and measurement setup and strategy and test and measurements results.
Keywords	test, EMI, GALS
Confidentiality Level	Public
Name of Client:	EC
Distribution List:	GALAXY, EC, internet
Authorised by:	Milos Krstic
Issue:	1
Document ID:	D12
Total Number of Pages:	20
Contact Details:	<a href="mailto:krstic@ihp-microelectronics.com">krstic@ihp-microelectronics.com</a>



## TABLE OF CONTENTS

<b>1</b>	<b>INTRODUCTION .....</b>	<b>7</b>
<b>2</b>	<b>REFERENCES .....</b>	<b>8</b>
2.1	<b>ACRONYMS .....</b>	<b>8</b>
<b>3</b>	<b>TEST AND MEASUREMENT SETUP AND RESULTS - LOW EMI FFT PROCESSOR.</b>	<b>9</b>
3.1	<b>FFT SYSTEM STRUCTURE .....</b>	<b>9</b>
3.2	<b>FFT ALGORITHM AND ARCHITECTURE.....</b>	<b>9</b>
3.2.1	<b>System Partition .....</b>	<b>9</b>
3.2.2	<b>Clock Modulation.....</b>	<b>10</b>
3.3	<b>SIMULATION RESULTS .....</b>	<b>11</b>
3.4	<b>CHIP FLOORPLAN .....</b>	<b>12</b>
3.5	<b>TESTING STRATEGY FOR MEASURING EMI .....</b>	<b>13</b>
3.6	<b>FUNCTIONAL TESTING.....</b>	<b>14</b>
3.7	<b>OPERATING FREQUENCY.....</b>	<b>15</b>
3.8	<b>POWER-MEASUREMENT.....</b>	<b>15</b>
3.9	<b>EMI-MEASUREMENT.....</b>	<b>15</b>
<b>4</b>	<b>TEST AND MEASUREMENT - PLL CIRCUIT .....</b>	<b>18</b>

## LIST OF FIGURES

Figure 1:	GALS FFT Processor.....	9
Figure 2:	Current Profile of four synchronous blocks.....	10
Figure 3:	Triangular modulation of clock frequency.....	11
Figure 4:	Comparison in current spectrum with MATLAB simulation .....	12
Figure 5:	FFT Test chip die photo .....	12
Figure 6:	Test chip bond plan.....	13
Figure 7:	Peering Vdd_core supply line .....	14
Figure 8:	Spectrum of the Vdd in I. Synchronous mode, II. Synchronous mode with clock jitter, III. GALS mode, and VI. GALS mode with clock jitter.....	16
Figure 9:	Reduction in the spectral peaks at p-th clock harmonics .....	17
Figure 10:	Chip and detailed circuit layout .....	18
Figure 11:	PCB of the test chip .....	19
Figure 12:	PCB and test setup of the chip.....	20



# GALAXY

GALS InterfAce for CompleX Digital  
SYstem Integration

Confid. Level: Public  
Date : 31/07/2009  
Issue: 1

---

## LIST OF TABLES

Table 1:	GALS System Partition.....	10
Table 2:	Clock Phase Modulation.....	10
Table 3:	Operating frequency configuration.....	15
Table 4:	Average operating current.....	15
Table 5:	Dependence of power consumption on the operating frequency.....	19



# GALAXY

GALS InterfAce for CompleX Digital  
SYstem Integration

Confid. Level: Public  
Date : 31/07/2009  
Issue: 1

---

## 1 INTRODUCTION

---

This document contains the description of the process of testing and measurement of our test chips designed to evaluate the advantages of GALS methodology.

In the run in February 2009 we have taped-out two different test chips:

- Low-EMI FFT processor (IHP)
- PLL circuit (EPFL)

In the following text we will discuss the results of the testing and measurement of those two chips.



# GALAXY

GALS InterfAce for CompleX Digital  
SYstem Integration

Confid. Level: Public  
Date : 31/07/2009  
Issue: 1

---

## 2 REFERENCES

---

### 2.1 ACRONYMS

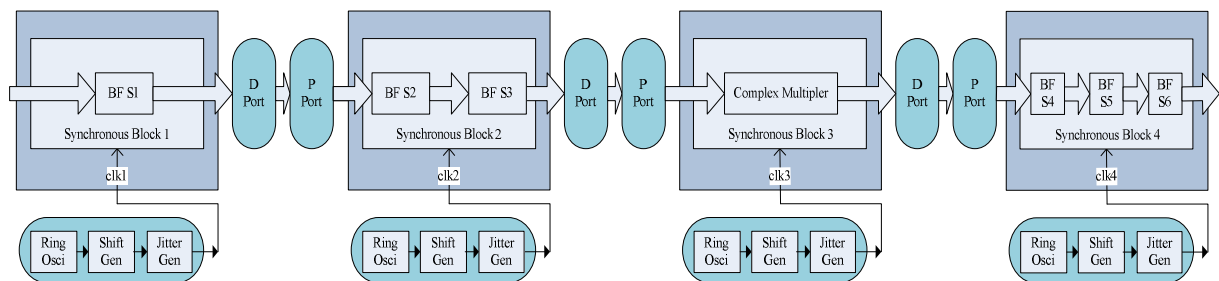
<b>GALS</b>	Globally Asynchronous Locally Synchronous
<b>EMI</b>	Electro-Magnetic Interference



### 3 TEST AND MEASUREMENT SETUP AND RESULTS - LOW EMI FFT PROCESSOR

#### 3.1 FFT SYSTEM STRUCTURE

The block diagram of the pipelined 64-point GALS FFT processor is shown in Fig. 1. To minimize the hardware complexity, the 64-point FFT is divided and conquered by two cascaded 8-point FFT computation. For each 8-point FFT, the novel Radix-23 FFT algorithm is developed and utilized, which has 3 stages of the butterfly (BF) structure. Based on this architecture, only one complex twiddle factor multiplier is required to perform pipelined 64-point FFT.



**Figure 1: GALS FFT Processor**

#### 3.2 FFT ALGORITHM AND ARCHITECTURE

To reduce the electromagnetic interference (EMI) of the digital circuits, in particularly the power and ground bounce caused by the simultaneous switching noise (SSN), which is critical for analog/digital mixed circuits design, the pausable clocking based GALS design is implemented as shown in Fig. 19. Each synchronous block is surrounded by an asynchronous wrapper, which consists of a local clock generator and a number of asynchronous I/O ports. By exploring the clock modulation on each block, significantly reduction in the sharp peaks of the system supply current, and consequently the bounce on the power and ground rings, can be expected.

##### 3.2.1 System Partition

There are totally seven functional sub-modules in the pipelined 64-point FFT processor, including six butterfly structures and one complex multiplier. To reduce the peaks on supply current, these sub-modules have been grouped and partitioned into four synchronous blocks according to the power and current consumption. To estimate the power consumption accurately, the dynamic power analysis is performed based on the simulation waveforms of the synthesized netlist using the IHP 0.13 $\mu$ m CMOS standard cells library. Tab. 1 presents the partition scheme of the GALS FFT processor, where each block has the similar contribution to the system power and current consumption.



	Sync. Block 1	Sync. Block 2	Sync. Block 3	Sync. Block 4
Function	BF Stage 1	BF Stage 2/3	Complex Mult.	BF Stage 4/5/6
Area <sup>(1)</sup>	38556 $\mu\text{m}^2$	46119 $\mu\text{m}^2$	47459 $\mu\text{m}^2$	40547 $\mu\text{m}^2$
Number of FF	651	637	173	362
Average power <sup>(2)</sup>	1.2mW	1.5mW	1.2mW	1.7mW
Average current	1mA	1.25mA	1mA	1.4mA

Note: (1) Reported by Synopsys DesignCompiler;

(2) Reported by Synopsys PrimeTime at 80MHz working frequency.

**Table 1: GALS System Partition**

### 3.2.2 Clock Modulation

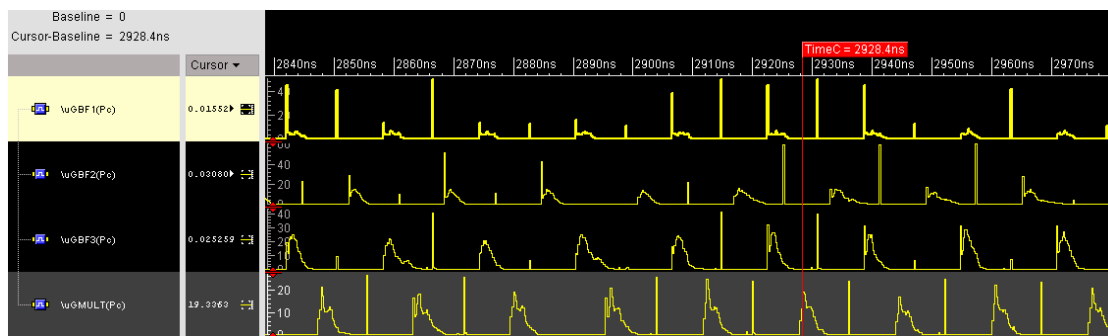
Two techniques of the clock modulation, phase modulation and frequency modulation, have been applied to the pausable local clock signals of four synchronous blocks.

#### Phase Modulation

For each pausable clock generator, its output clock is first propagated through a programmable delay line. By programming the delay line, the rising edge of each clock can be shifted independently. These clock shifting results in the spread on the switching activities of the synchronous blocks, and therefore, the sharp peaks on the system supply current will be reduced substantially. In the experiment, the clock signals of four synchronous blocks are shifted and evenly allocated within the clock period, as shown in Tab. 2. For instance, the evenly distribution of supply currents of four synchronous blocks is clearly illustrated in Fig. 2.

	Sync. Block 1	Sync. Block 2	Sync. Block 3	Sync. Block 4
$t_{CLK+}$	0	$T_{CLK}/4$	$T_{CLK}/2$	$3T_{CLK}/4$

**Table 2: Clock Phase Modulation**



**Figure 2: Current Profile of four synchronous blocks**

Phase modulation is also applied on the traditional synchronous design to re-shape the supply current, where the intended clock latency and clock skew are introduced in the global clock tree networks to spread switching activities. However, due to the setup-time and hold-time constraints, the clock phase modulation is restricted in a rather small range (typically less than 5%TCLK). On the contrary, attributed to the asynchronous communication between blocks in the GALS design, there is no constraint on the phase modulation of synchronous blocks (25%TCLK in the experiment for example). It means that phase modulation can be optimized in terms of minimum peaks on current in GALS designs.



### Frequency Modulation

Another approach to reduce EMI/SSN is to randomize the working frequency of the digital circuits, which spreads the supply current in spectrum. In the experiment, clock jitter is introduced to modulate its frequency. Fig. 3 depicts a jitter generator and the corresponding clock period variation. The output clock from the phase modulator is propagated through a set of delay lines with different length, and a multiplex is employed to select a delay version of the input clock as the output clock. Simply changing the control coding scheme of the multiplex, we can modulate the clock jitter in diverse modes using this structure, such as linear modulation or pseudo-random modulation. However, to achieve different jitter modes, the control coding scheme needs to be designed carefully to avoid any potential glitch on the output clock. The single-hot coding is utilized to modulate the clock in a triangular (linear) mode, in which the clock period  $T_{CLK}$  changes from  $(T_{CLK}-4DELTA)$  to  $(T_{CLK}+4DELTA)$  with a modulating granularity  $DELTA=0.15ns$ . To further randomize the frequency of the system, four local clocks are initialized with different offsets on  $T_{CLK}$ .

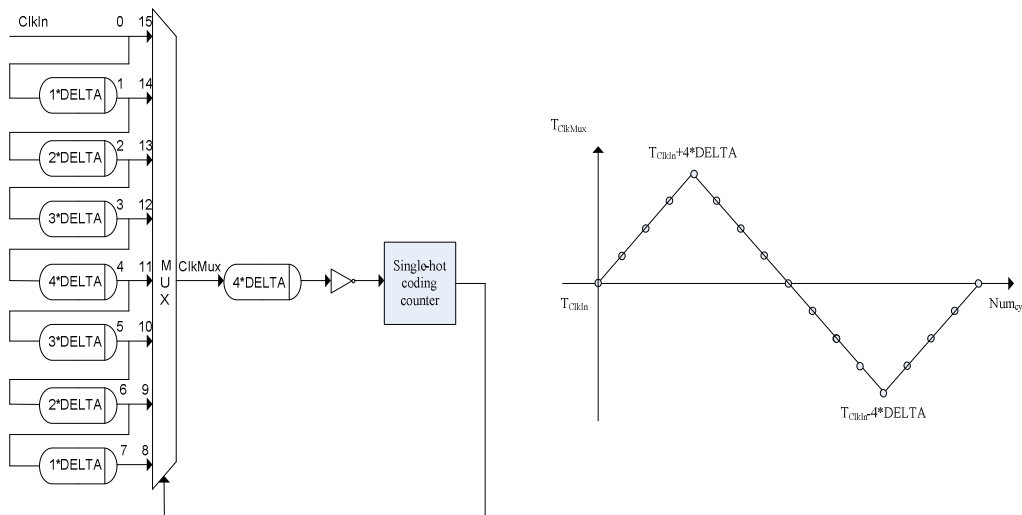
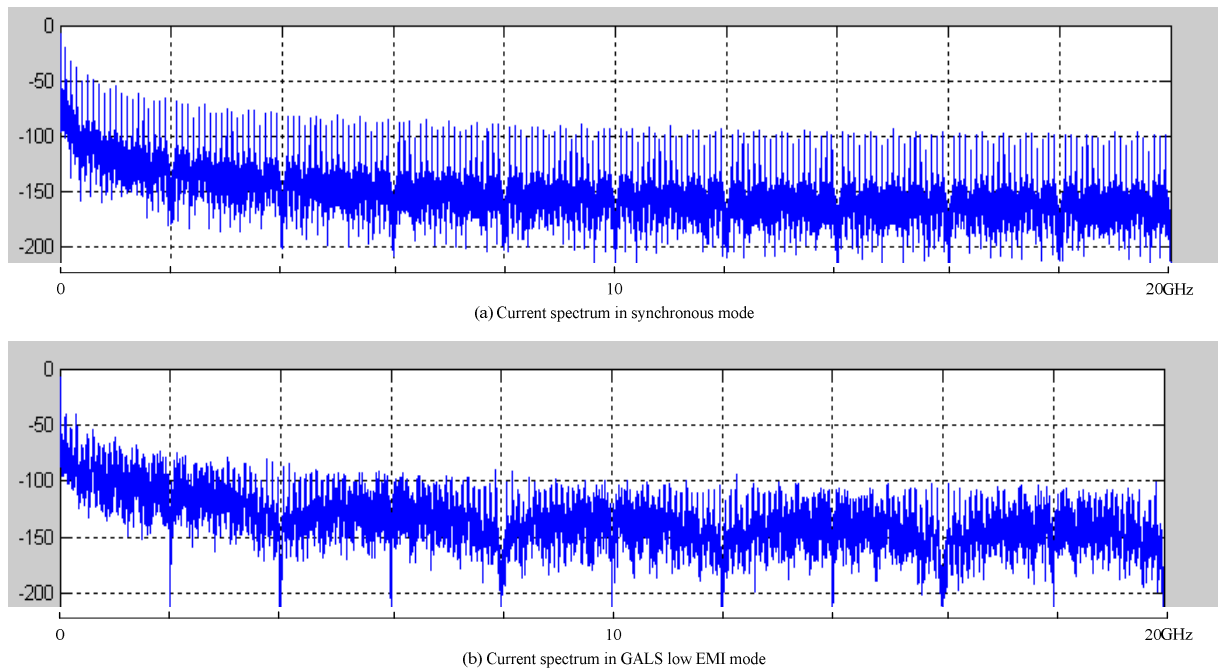


Figure 3: Triangular modulation of clock frequency

### 3.3 SIMULATION RESULTS

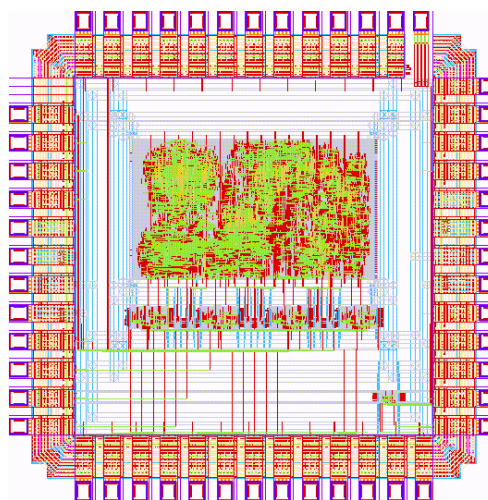
To compare the performance of synchronous FFT and GALS FFT in terms of EMI/SSN, we develop a test model in MATLAB. The information about system partition and clock modulation on each block is used in the model to generate the current profile. Fig. 4 presents a comparison in the spectrum of supply current from 0 to 20GHz in two modes. It can be observed there is an in average more than 10dB attenuation in the frequency domain by utilizing clock modulation based on GALS design with respect to the traditional synchronous design.



**Figure 4: Comparison in current spectrum with MATLAB simulation**

### 3.4 CHIP FLOORPLAN

In order to reduce the cost of the testing but to enable on-wafer measurement we decided to use already existing needle-card. However, in order to utilize this card we have to adapt our chip floorplan to this needle card. The die photo of the test chip is given on Fig. 5. Chip size is  $1.73 \times 1.73 = 3 \text{ mm}^2$ . The number of data pins is 43 and there are 8 power and ground pins (2 Vddcore, 2 Gndcore, 2 Vddpad, 2 GNDpad).



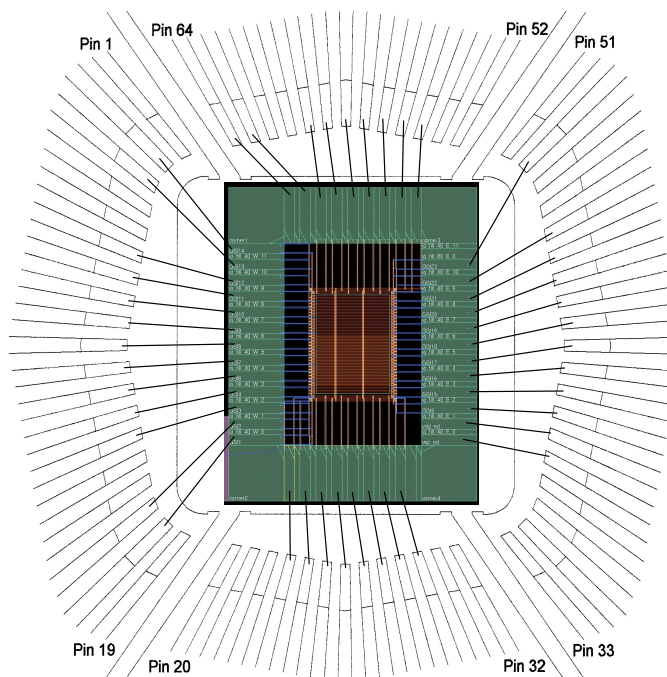
**Figure 5: FFT Test chip die photo**



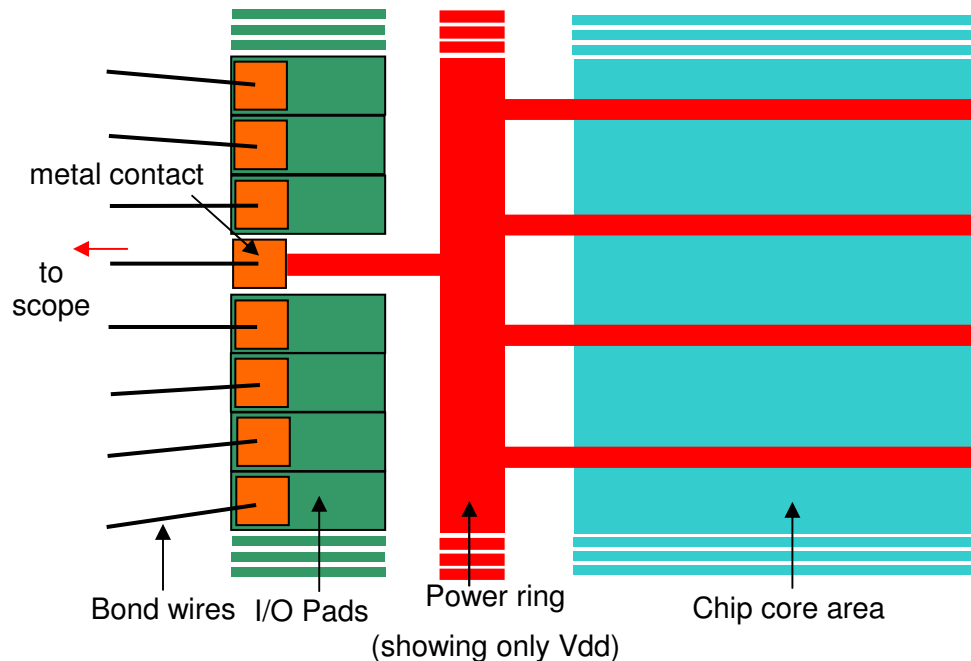
## 3.5 TESTING STRATEGY FOR MEASURING EMI

It is very difficult to measure the EMI and current profile using the hardware tester. Normally, the access to the power pins is very limited and large capacitance is placed there to prevent any voltage drop on power lines. Therefore, we have decided to generate the special strategy for EMI evaluation during test. For the test and measurement the following strategy is used:

- Since this test chip contains several cores it is very important that it is possible to disable the dynamic power consumption of the cores that are not subject to EMI testing.
- Functional verification and test can be performed with on-wafer testing. However, due to the difficult access to the pins for scope and no support from the tester side, EMI-measurement is difficult, not-reliable, or even not possible.
- Applied process (130 nm CMOS from IHP) has dual power supply for core and for pads. Therefore, it is not possible by tracking of normal I/O pads to get the access to the core supply changes.
- EMI measurement could be best performed after packaging of the test chip. For this we can use the standard package QPF64. The bond-plan is given on Fig.6.
- In order to enable evaluation of power profile we had to design special test probe board. This board has to enable the following functions: switching on/off the capacitors on the power lines, routing of the power lines to SMA connectors where the power profile can be observed over oscilloscope/ spectrum analyzer.
- One special pad in design will be dedicated to peering of the power supply. This pad will be directly connected to internal power ring. We will enable scoping of this pad directly and independently from other power pads. This pad will not be directly routed on board to the other power pad and to power supply. Simplified diagram of this structure is shown in Fig. 7.



**Figure 6: Test chip bond plan**



**Figure 7: Peering Vdd\_core supply line**

### 3.6 FUNCTIONAL TESTING

The produced and packaged chip was tested on CertiMAX test platform provided from IHP. The following tests are performed:

- Standard continuity test of the pads
- Standard Short/Open Circuit Test
- Internal Clock Generator test - we have placed one additional clock generator based on the ring oscillator and we have tested its operation (clock generation, clock pausing, clock stopping). This clock generator contains also special standard cells (C-element, Mutex) that are specially developed for GALAXY project. The goal of this test is first to test the technology performance and additionally to test on-chip developed standard cells and their functionality.
- Idle Test of FFT Chip - In this test the complete chip is in idle (reset) mode. The goal is to evaluate that stand-by current is acceptable and to verify EMI-behaviour of non-active circuit.
- Synchronous FFT operation - In this mode we have standard synchronous operation of the FFT processor.
- Synchronous FFT with jitter - In this mode we have standard synchronous operation of the FFT processor with added jitter to clock source.
- GALS FFT operation - FFT operation in GALS mode. FFT is divided into 4 different LS modules which communicate asynchronously. LS modules are driven by local clock generators based on the pausable clocking.
- GALS FFT operation with added additional skew between the blocks - FFT operation in GALS mode. FFT is divided into 4 different LS modules which communicate asynchronously. LS modules are driven by local clock generators based on the pausable clocking. Between modules we add special programmable delay lines to insert the timing skew in the operation.



- GALS FFT operation with added jitter - FFT operation in GALS mode. FFT is divided into 4 different LS modules which communicate asynchronously. LS modules are driven by local clock generators based on the pausable clocking. All pausable clocks are extended with additional jitter generator to insert the jitter on the clock line.
- GALS FFT operation with added jitter and skew - This is a combined test where we apply both methods for EMI reduction.

All functional FFT tests were based on the BIST testing and this was our monitor to see the successfulness of each test. FFT chips are tested for all those tests and we have identified the chips where all tests were successful. Those chips were further used for EMI measurement and evaluation.

### 3.7 OPERATING FREQUENCY

In GALS modes, the internal clocks are generated by the ring oscillators, which working frequencies are controlled by the configure signal CC\_FFT[4:0]. As shown in Table 3, we measured all the frequencies at which the chip works correctly. We see that the highest working frequency in GALS modes is about 90MHz.

CC_FFT [4:0]	10100	10101	10110	10111	11000	11001
<i>Freq (MHz)</i>	<i>88.4375</i>	<i>85.625</i>	<i>81.875</i>	<i>79.0625</i>	<i>76.25</i>	<i>73.4375</i>
CC_FFT [4:0]	11010	11011	11100	11101	11110	11111
<i>Freq. (MHz)</i>	<i>71.5625</i>	<i>68.875</i>	<i>66.875</i>	<i>65</i>	<i>63.125</i>	<i>61.25</i>

**Table 3: Operating frequency configuration**

### 3.8 POWER-MEASUREMENT

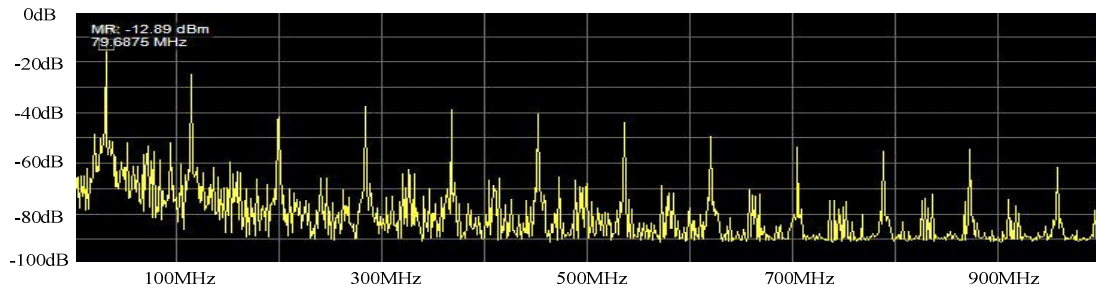
The average operating current reported by CertiMax testing machine is presented in Table 4, where the external clock used in Sync modes is 80MHz and the internal clocks used in GALS modes are also configured to be around 80MHz (CC\_FFT[4:0] is programmed to be 10111).

	S_N	S_J	G_N	G_S	G_J	G_SJ
<i>Pad (mA)</i>	<i>0.2</i>	<i>0.2</i>	<i>0.3</i>	<i>0.3</i>	<i>0.3</i>	<i>0.3</i>
<i>Core (mA)</i>	<i>14.1</i>	<i>14.1</i>	<i>12.7</i>	<i>12.7</i>	<i>14.7</i>	<i>14.7</i>

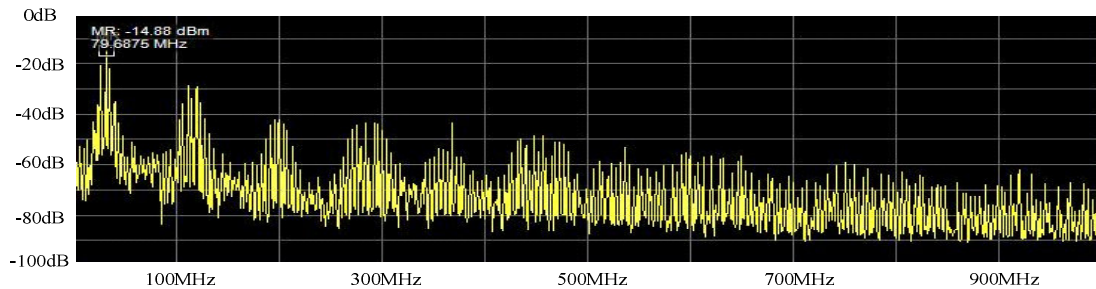
**Table 4: Average operating current**

### 3.9 EMI-MEASUREMENT

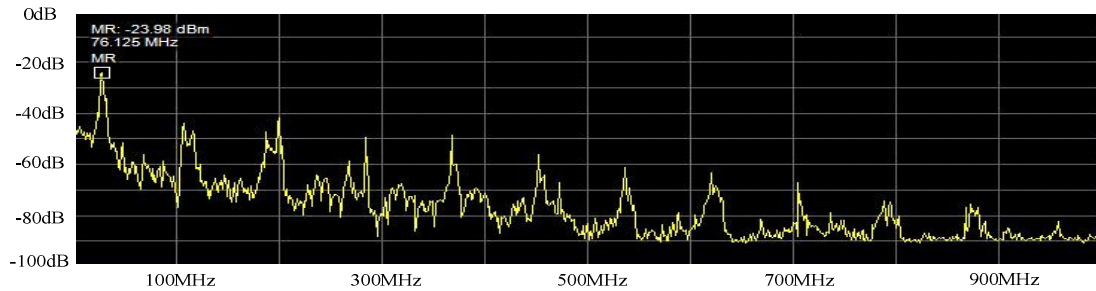
We have measured the supply voltage (Vdd) in frequency domain when the chip operated in different modes. The comparison in the spectra of the VDD is shown in Fig. 8, and the corresponding reduction in dB in the spectral peaks is shown in Fig. 9. For measurement we have used the strategy explained in section 3.5.



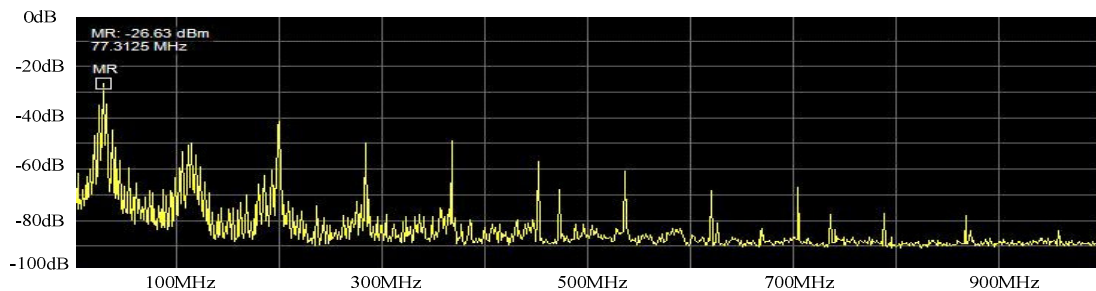
I Synchronous mode



II Synchronous mode with clock jitter



III GALS mode



VI GALS mode with clock jitter

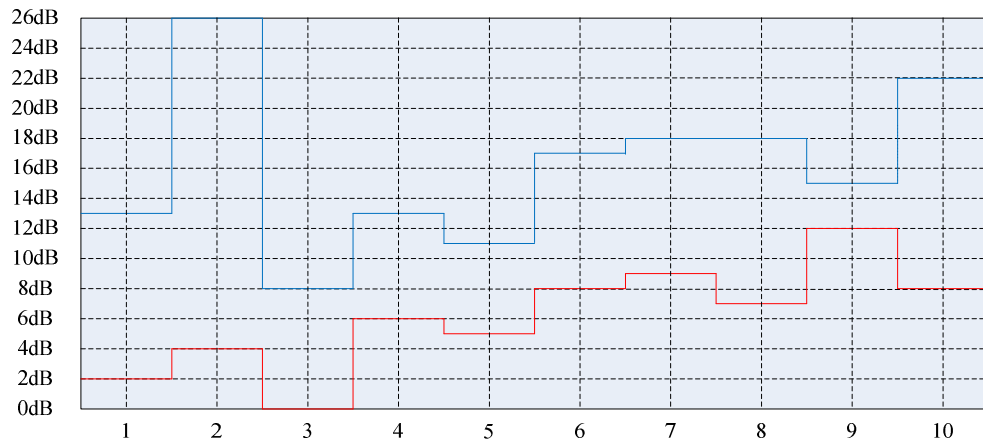
**Figure 8: Spectrum of the Vdd in I. Synchronous mode, II. Synchronous mode with clock jitter, III. GALS mode, and VI. GALS mode with clock jitter**



# GALAXY

GALS InterfAce for CompleX Digital  
SYstem Integration

Confid. Level: Public  
Date : 31/07/2009  
Issue: 1



**Figure 9: Reduction in the spectral peaks at p-th clock harmonics**

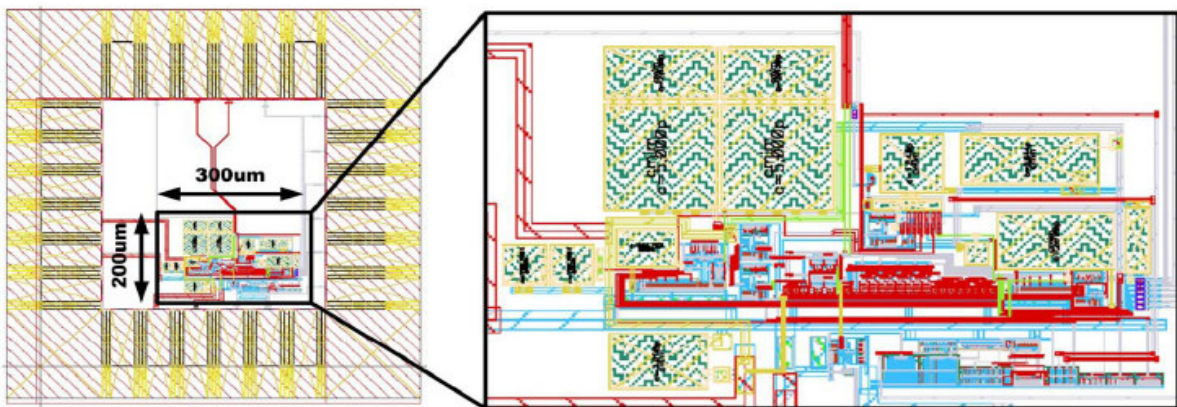
**(Red line: synchronous mode with clock jitter, Blue line: GALS mode with clock jitter)**



## 4 TEST AND MEASUREMENT - PLL CIRCUIT

Test chip has been designed and produced in order to evaluate low-power features of GALS methodology. The chip contains a low-power PLL-based clock generator that has a wide tuning range of 0.43-430kHz. The power consumption of the circuit is proportional to the output clock frequency. The VCO is implemented with a wide tuning range ring oscillator based on subthreshold delay. A widely adjustable loop filter has been used to implement the loop filter.

A screenshot of the whole chip and circuit layout are given in Fig. 10.



**Figure 10: Chip and detailed circuit layout**

The implemented PLL has the following characteristics:

- ◆ Tuning range:  $\times 1000$  [ 430Hz  $\rightarrow$  430kHz ]
- ◆ Bias current: 20pA  $\rightarrow$  20nA
- ◆ Scalable power consumption:  $\approx 250$ pW/Hz
- ◆ Very small area:  $200 \times 300 \mu\text{m} = 0.06 \text{mm}^2$

The power consumption is very small due to subthreshold operation and its dependence on the operation frequency should be linear. However, due to bias circuit's consumption power consumption is slightly increased for lower frequency range (430Hz to 43kHz). The ration of power consumption (total current consumption) to operating frequency is given in Table 5I.



# GALAXY

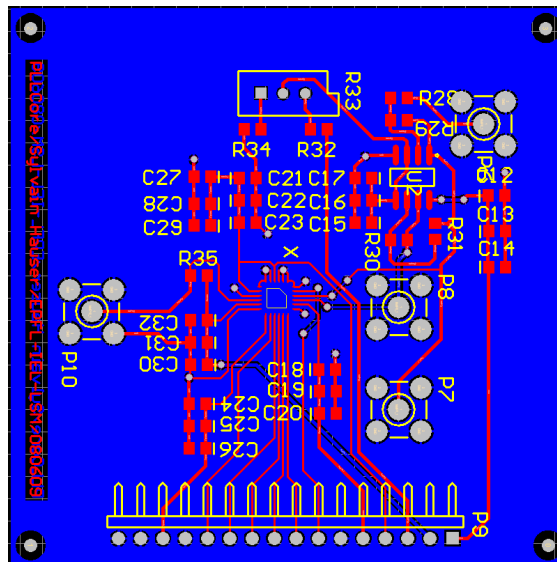
GALS InterfAce for CompleX Digital  
SYstem Integration

Confid. Level: Public  
Date : 31/07/2009  
Issue: 1

f [kHz]	I <sub>DD_RMS</sub> [μA]
0.43	0.28
4.3	0.91
43	2.7
430	21.1

**Table 5: Dependence of power consumption on the operating frequency**

After fabrication the dies were bonded to the prepared PCB shown in Fig. 11. The photos of PCB and test setup are depicted in Fig. 12.



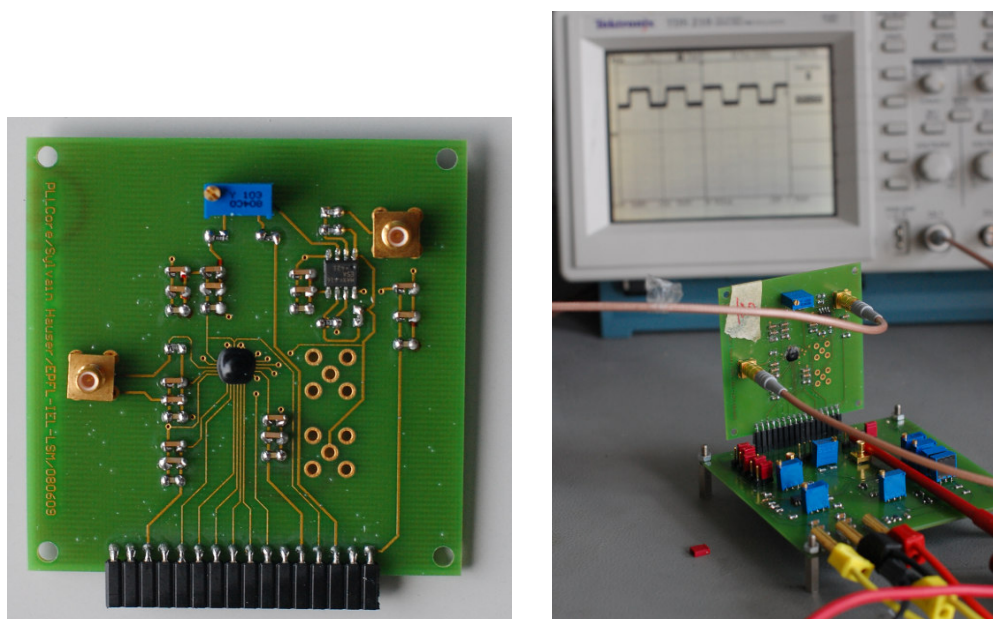
**Figure 11: PCB of the test chip**



# GALAXY

GALS InterfAce for CompleX Digital  
SYstem Integration

Confid. Level: Public  
Date : 31/07/2009  
Issue: 1



**Figure 12: PCB and test setup of the chip.**

The chip has been measured and it has been shown that it is fully operational in the frequency range of 600Hz to 300kHz. With careful tuning of the bias current the operating range can be adjusted to be close to the designed one (430Hz to 430kHz).