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In this report we will provide the results of the testing and measurements of the second test chip designed to evaluate the advantages of GALS design. This text consists of two parts: test and measurement setup and strategy and test and measurements results.

Keyword list: asynchronous design, chip fabrication, GALS, low power design, variability

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1 INTRODUCTION

This document contains the description of the process of testing and measurement of the second test chip designed to evaluate the advantages of GALS methodology.

In the run in August 2009 we have taped-out a test chips with two different designs:

- Power switch for dynamic voltage scaling (DVS) scheme
- Local variability testing circuits

In the following text we will discuss the results of the testing and measurement of those two designs.

2 REFERENCES

2.1 ACRONYMS

ABB	Adaptive Body Biasing
AES	Advanced Encryption Standard
DVS	Dynamic Voltage Scaling
DVFS	Dynamic Voltage-Frequency Scaling
GALS	Globally Asynchronous Locally Synchronous
WID	Within-die

3 TEST AND MEASURMENT SETUP

3.1 GLOBAL CHIP STRUCTURE

The implemented test chip includes two types of test structures.

3.1.1 Power switch test structure

The first test structure implemented on the chip is a power switch designed to smoothly switch between two supply voltages (in our case nominal 1.2V and secondary supply – default of 0.8V) as a part of dynamic voltage scaling scheme. The switch has been design in the form of supply ring which provides distributed supply. This is to test power switch design for the DVS scheme on the realistic example. The switch has also the appropriate driver. The simulated characteristics are 50ns transition time for 10mA pick current dynamic load. This load is an AES 128b cryptographic core.

The AES 128b block diagram is shown in Fig. 1.

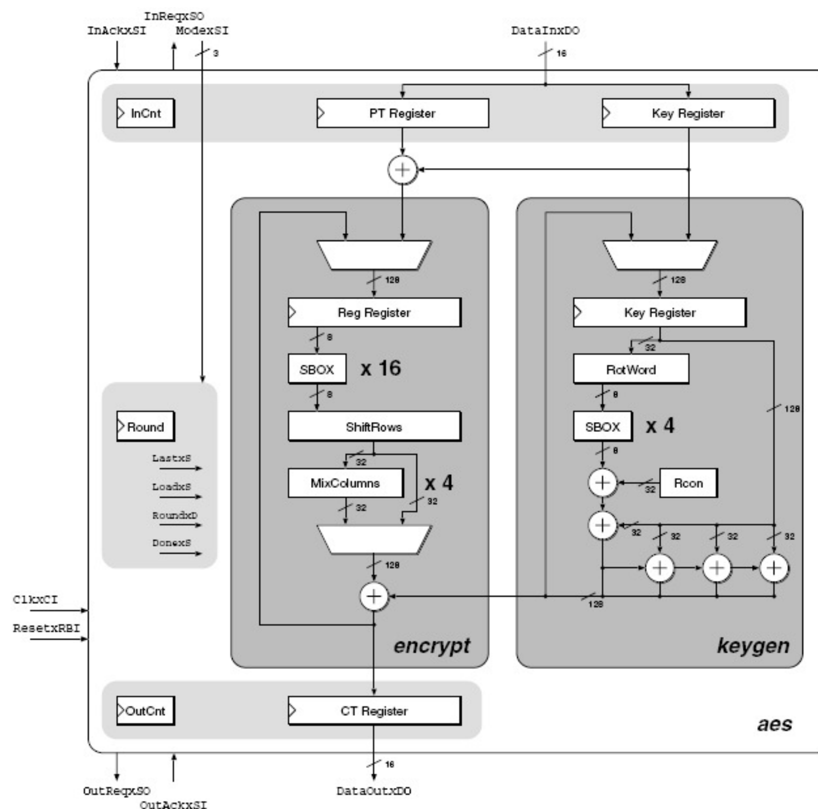

Figure 1: AES 128b cryptography core.

The chosen design is suitable for GALS partitioning (two to three partitions) as well as for DVS scheme application. In DVS application, a control block would dynamically apply policies for switching between two operating voltages according to desired workload.

Simulation results

The target operating frequency of the AES core is 200MHz. The typical power consumption and maximum operating frequency of AES core (as reported by Synopsis PrimeTime and DesignCompiler) are 5.2mW (at 200MHz) and 320MHz. The leakage power (total power while clock is not active) is 0.3mW.

The simulated values of transition times (defined from 20-80% of value) for rising and falling edge with the given AES core as a load for 1.2V nominal voltage and different values of secondary power supply are given in Table 1. The values are very small compared to a target clock period enabling the use of aggressive DVS policy (switching to lower power supply for any period of reduced activity longer than 1µs).

Table 1: Transition times for various supply voltages

V_{DD2} [V]	$t_{tran,r}$ [ns]	$t_{tran,f}$ [ns]
0.6	45	35
0.8	30	20
1.0	18	12

3.1.2 Ring oscillators test structure

The second test structure consists of 6 groups of ring oscillators different in number of stages (namely 5, 7, 9, 11, 13 and 15). Each group contains 100 ring oscillators of the same size and frequency, divider and decoder used to measure operating frequencies. Since all the oscillators are present on the same die but spread all over the chip the test structure is very suitable for local variations – within-die (WID) variations measurement. The local variability can be characterized, and standard deviation of local variability for a gate and circuit - sigma_gate and sigma_circuit, can be derived. Moreover, we can also exactly determine spatial correlation coefficient for local variations which is a novel contribution.

The WID variations model represents systematic within-die parameter variations by expressing the device-to-device correlation as a function of the distance between the devices. This correlation function, however, is significantly influenced by specific manufacturing capabilities. For future technology nodes relatively smaller gate to gate correlation factors are expected, considering that wire connections are not scaling with the same factor as transistors sizes which makes gate to gate transistor distances relatively larger with respect to previous technologies.

To simplify the analysis, two separate WID variations cases can be indentified: 1) completely dependent gates (gate delay correlation equal to 1) and 2) completely independent gates (gate delay correlation equal to 0), which may be viewed as extreme conditions of systematic and random variations, respectively.

In the completely systematic case, the variations have the same impact on every element in a critical path:

$$\frac{\sigma_{T_{cp}}}{T_{cp}} = \frac{n_{cp}\sigma_{T_{inv}}}{n_{cp}T_{inv}} = \frac{\sigma_{T_{inv}}}{T_{inv}} \quad (1)$$

where σ_{Tcp} and σ_{Tinv} are the standard deviations of the ring oscillator delay distribution and the inverter gate delay distribution, respectively; n_{cp} is the number of ring oscillators; T_{inv} and T_{cp} are critical path and inverter gate delay, respectively. This case, however, is not realistic in state-of-the-art technology nodes, where distance between transistor gates relative to transistor sizes is increasing with respect to scaling.

In the case of completely random variations, however, the variations in the critical path delay are expected to have an averaging effect over the gates in the path:

$$\frac{\sigma_{T_{cp}}}{T_{cp}} = \frac{\sigma_{T_{inv}}}{\sqrt{n_{cp}}T_{inv}} \quad (2)$$

For completely random WID variations, the ratio of standard deviation to mean for the delay of the critical path is inversely proportional to the square root of number of stages (n_{cp}). This is a more realistic approximation of the circuit delay variations in state-of-the-art technology nodes than (1).

In general case variance of the sum of n_{cp} identical random variables (X_1, … , X_n) is given with

$$\mathrm{Var}\left(\sum_{i=1}^{n_{cp}} X_i\right) = \sum_{i=1}^{n_{cp}} \mathrm{Var}(X_i) + 2\sum_{i=1}^{n_{cp}-1}\sum_{j=i+1}^{n_{cp}} \sqrt{\mathrm{Var}(X_i)\mathrm{Var}(X_j)}\,\rho(X_i, X_j) \quad (3)$$

where $\rho(X_i, X_j)$ is a correlation factor between random variables X_i and X_j. If (3) is applied to gates in the critical path, $\mathrm{Var}(X_i)$ becomes σ^2_{Tinv} for every gate, $\mathrm{Var}\left(\sum_{i=1}^{n_{cp}} X_i\right)$ becomes σ^2_{Tcp} and $\rho(X_i, X_j)$ becomes $\rho_{i,j}$ – correlation factor between ith and jth gate in the critical path. With these substitutions (3) becomes

$$\sigma^2_{T_{cp}} = n_{cp}\sigma^2_{T_{inv}} + \sigma^2_{T_{inv}} \times \sum_{i=1}^{n_{cp}-1}\sum_{j=i+1}^{n_{cp}} \rho_{i,j} \quad (4)$$

After dividing (4) with T_{cp},

$$\frac{\sigma_{T_{cp}}}{T_{cp}} = \frac{\sigma_{T_{inv}}}{\sqrt{n_{cp}}T_{inv}} \sqrt{1 + \frac{2}{n_{cp}} \sum_{i=1}^{n_{cp}-1}\sum_{j=i+1}^{n_{cp}} \rho_{i,j}} \quad (5)$$

In case $\rho_{i,j}$=1 for any pair of gates (5) becomes (1), otherwise for $\rho_{i,j}$=0 for any pair of gates (5) becomes (2). Due to the difference in their physical origins, variations of L and V_{th} exhibit different characteristics of correlation among transistors: lithography induced variation of L is spatially correlated, while V_{th} variation is mostly random due to dopant fluctuations.

For a small-size gate, strong correlation is usually assumed to reduce the complexity of analysis. However, for a realistic circuit path that spans across larger distances, knowing spatial correlation among gates is important for accurate statistical timing analysis. A spatial correlation can be modelled as a linear function of distance. Here we are using the following simplified model:

$$\rho_{i,j} = \begin{cases} \rho_0 (1 - \frac{j-i-1}{D}) & \text{for} \quad j\text{-}i \le D \\ 0 & \text{for} \quad j\text{-}i > D \end{cases} \tag{6}$$

where ρ_0 is the correlation factor between neighbouring gates (j=i+1) and D is the maximum distance between gates where correlation effects are still present. A spatial correlation model from (6) is illustrated in Fig. 2.

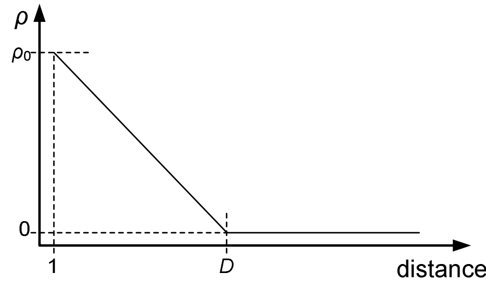

Figure 2: Spatial correlation modelled as a liner function of distance.

Substituting (6) into (5) with assumption that $n_{cp} \le D+2$ yields:

$$\rho_0 = \frac{\left(\frac{\sigma_{T_{cp}} T_{inv}}{T_{cp} \sigma_{T_{inv}}}\right)^2 n_{cp} - 1}{(n_{cp} - 1)\left(1 - \frac{n_{cp} - 2}{3D}\right)} \tag{7}$$

Eq. (7) has two parameters, ρ_0 and D that need to be estimated for the given technology using the measured results.

Self tuning ring oscillators can be used in dynamic frequency-voltage scaling (DVFS) scheme. The idea would be to use ring oscillators locally in different portions of the chip to determine maximum operating frequency for each synchronous block. More precisely, to use ring oscillators as the feedback for local clock generators in order to have each local synchronous module operating at maximum possible frequency.

3.2 Chip Floorplan

The chip on its own is 1.52 x 1.52 = 2.31 mm^2 with 34 data and 14 power pins, and is designed in 130 nm CMOS process provided from IHP. This number of pins is high due to two independent test structures that are implemented on the chip. The core area is 1.05 x 1.05 = 1.1 mm^2. In Fig. 2 we have shown the pad diagram of the chip.

Device Pinout

(CHIP EXTENT: 1050um X 1050um)

Top side:

48	47	46	45	44	43	42	41	40	39	38	37
VDDIO	InxDI[0]	InxDI[1]	InxDI[2]	InxDI[3]	VSS_1	VDD_H1	VDD_L	InxDI[4]	InxDI[5]	InxDI[6]	InxDI[7]

Left and right sides:

Pin	Name	Name	Pin
1	VSS_RING1	VSS_RING4	36
2	VDD_RING1	VDD_RING4	35
3	SEL_CLK	VDD_INT	34
4	SEL_IN	SH	33
5	CNT_EN	SL	32
6	READ_EN	StrobexSI	31
7	CNT_OUT	ReadyxSO	30
8	CNT_CLK	LoadxSI[0]	29
9	RING_OUT	LoadxSI[1]	28
10	RST	ResetxRBI	27
11	VDD_RING2	VDD_RING3	26
12	VSS_RING2	VSS_RING3	25

Bottom side:

OutxDO[0]	OutxDO[1]	OutxDO[2]	OutxDO[3]	OutxDO[4]	OutxDO[5]	VSS_2	VDD_H2	OutxDO[6]	OutxDO[7]	ClkxCI	VSSIO
13	14	15	16	17	18	19	20	21	22	23	24

Figure 3: Test chip pad diagram.

In Fig. 3 a screenshot of circuit layout and chip photo are shown.

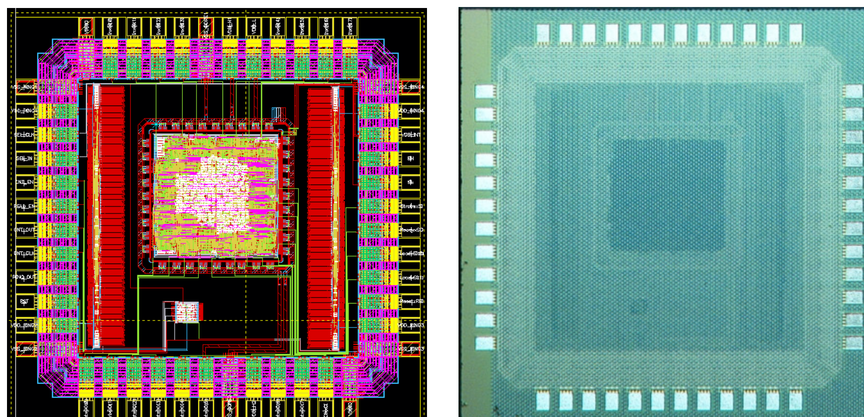

Figure 4: A screenshot of the circuit layout and chip photo.

The chip is using analogue pads since the operating frequency of digital pads is limited to 100MHz.

3.3 MEASUREMENTS SETUP

Two boards have been designed. First board (depicted in Fig. 4) was used for chip-on-board mounting and contains only power lines capacitors, standard pin connectors and an additional connector that is used to access the special pad in design dedicated to peering of the power supply. This pad is directly connected to internal power ring.

The second PCB contains all the additional necessary circuitry. Since analogue pads are used on the chip, an appropriate driver circuit has to be used. MAX4220, 200MHz -3dB bandwidth, 600V/µs, low input cap (1pF) op-amps have been used as output drivers from the circuit. The op-amps are design in feedback loop with variable gain set to +2 by default. This way the output is in the range of 0-2V. The outputs are then driven to Agilent 16702 logic analyser system. The pattern generator of the same logic analyser system is used to generate appropriate input signals.

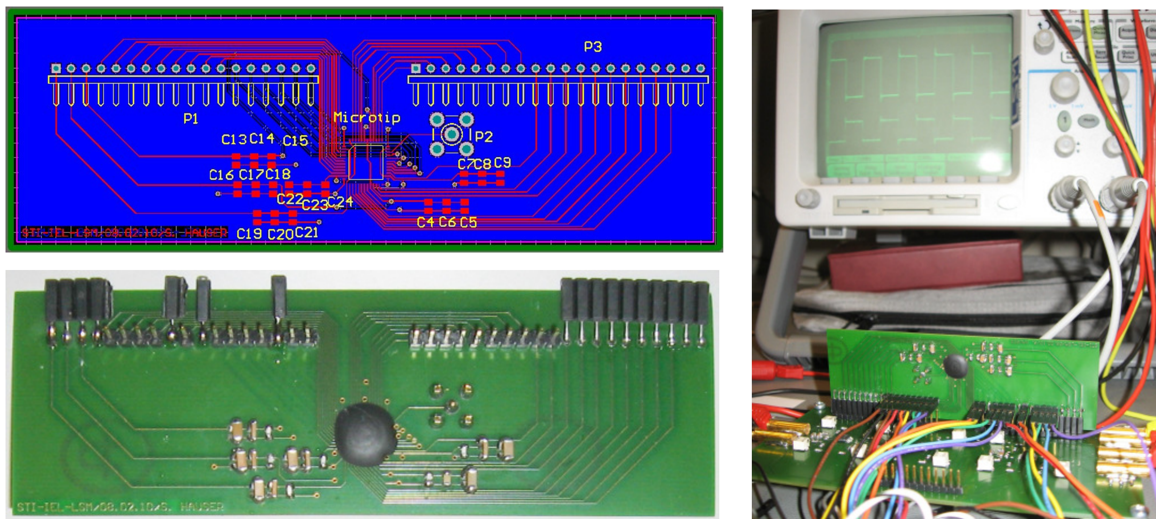

Figure 5: PCB and test setup of the chip.

Functional testing has been performed and the functionality of the AES core has been confirmed using standard test AES test patterns.

3.4 MEASUREMENTS RESULTS

3.4.1 Power switch test structure

Switching transition times, dynamic and leakage power dissipation and maximum operating frequency for different supply voltages have been measured.

Measured switching times (Table 2) show good accordance with simulation times and confirm that an aggressive DVS policy can be used. 0.6V is the lowest tested supply voltage that allows correct operation since the chip doesn't contain any level shifters.

Table 2: Transition times for various supply voltages

V_{DD2} [V]	$t_{tran,r}$ [ns]	$t_{tran,f}$ [ns]
0.6	50	32
0.8	34	18
1.0	20	10

Dynamic and leakage power dissipation (Table 3) show large reduction for lower voltages. Dynamic power dissipation is measured at 40MHz clock speed since at 0.6V the circuit cannot operate at higher frequency. The total power dissipation at 0.6V supply voltage is only 0.42mW.

Table 3: Dynamic and leakage power for various supply voltages

V_{DD2} [V]	P_{dyn} [mW]	P_{leak} [mW]
0.6	0.3	0.12
0.8	0.5	0.18
1.0	0.8	0.25
1.2	1.1	0.35

The maximum operating frequency of the circuit is also measured for various supply voltages. The clock speed is increased until the moment the first incorrect output vector is registered. For nominal supply voltage of 1.2V the maximum operating frequency is limited with the speed of op-amps used for driving the output signals and is much higher than 200MHz. Therefore, this point is not considered. The other values are given in Table 4.

Table 4: Transition times for various supply voltages

V_{DD2} [V]	$f_{clk,max}$ [MHz]
0.6	40
0.8	130
1.0	230

Significant reduction in power dissipation for lower supply suggest once again possibility for aggressive DVS policy and potential for running different local islands in GALS architecture on different (lower) supply voltages (than the nominal).

3.4.2 Ring oscillators test structure

The operating frequency of ring oscillators have been measured for various ring oscillator stages (5, 7, 9, 11, 13 and 15) and for two operating voltage, nominal (1.2V) and 0.6V. In Fig. 5 normalized (divided by the mean value) distribution of operating frequency for 5 stages ring oscillator and both operating voltages (1.2V and 0.6V) is shown. It can be seen that for 0.6V supply voltage the distribution is wider – the standard deviation is larger.

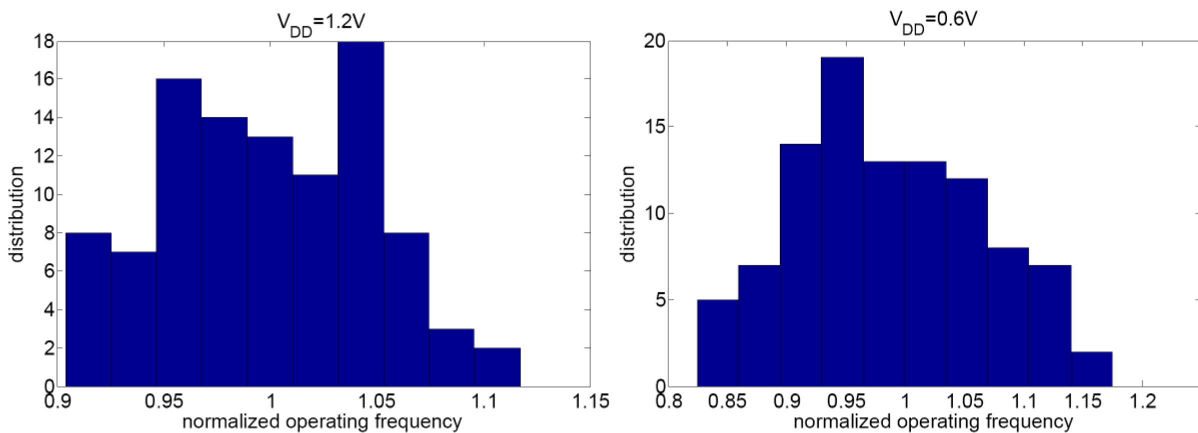

Figure 6: Distribution of normalized operating frequencies.

In Table 5 values of normalized standard distribution for both operating voltages and different number of stages is shown.

Table 5: Normalized standard deviation of ring oscillator operating frequency

Num. of stages	V_{DD}=1.2V	V_{DD}=0.6V
5	4.8%	8.3%
7	4.0%	6.9%
9	3.45%	6.0%
11	3.1%	5.35%
13	2.8%	4.85%
15	2.6%	4.45%

As it can be seen from the table the variability (standard deviation) almost doubles when the supply voltage is 0.6V. This enhances the need for variability impact reduction methods. Since all the measurements are from the same die the variations are exclusively local (WID). Therefore, the methods such as adaptive body biasing (ABB) and DVS do not produce sufficient results.

One more characteristic that has been extracted from the measured results is the spatial correlation coefficient for local variations. After applying the linear fitting to (7) using the values for local variations from Table 5, the following values are acquired (95% confidence parameter interval in brackets) **ρ_0=0.17 (0.10-0.22)** and ***D*=5 (3.9-6.1)**. Such a low correlation factor even for neighbouring gates signifies that WID variations are mostly random. For distances larger than 5 inverter gates, which is equivalent to 10μm, there is zero correlation of WID variations.