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Keyword list: GALS, EMI, current profile
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1 INTRODUCTION

Rapid and continuous development of the process technologies and device miniaturization imposes enormous challenges on designers and CAD tools. The classical synchronous paradigm became very difficult to achieve due to the problems in clock tree generation and timing closure. For mixed digital-analog designs, the challenges are even harder. Analog systems are very sensitive to the noise introduced by the digital components. Therefore, additional methods must be used for lowering of EMI (Electromagnetic Interference). The GALS (Globally Asynchronous Locally Synchronous) methodology has been proposed as a solution for the system integration many years ago [MUT00]. There have been some proposals to use the GALS methodology also for EMI reduction [GR5]. It has been shown on several examples that asynchronous design can significantly reduce EMI in comparison to the classical synchronous design. One example is an asynchronous design of an ARM9 processor called Amulet 2 [FR99]. There are also some initial studies regarding the GALS approach for EMI reduction [GR5]. They have shown that the GALS systems can achieve EMI reduction up to 20 dB in comparison with a synchronous design. In time domain, the noise peaks can be lowered up to 40%. However, the real on-chip measurements [KGS05] have shown smaller EMI reduction.

Additionally, those activities were not systematic and have been focused only on specific design cases, not taking into consideration GALS as a general methodology for system integration. The technology advance and further device miniaturization increases a demand for deep investigation of EMI because of its detrimental influence on a whole system performance.

Moreover, there are no dedicated tools to model EMI in GALS and synchronous circuits on a high abstract level. It is needed to have the possibility to predict at least approximate values of EMI in designed digital systems. In synchronous systems, which are much more evaluated because of their wide application, it is easier to estimate EMI. There are many investigations showing the possibility of reduction of EMI in synchronous systems by adding clock skew and phase modulation of the clock [BL04, BA06]. However, adding a clock skew or a phase modulation of a clock to a synchronous chip demands additional work and sometimes generates very difficult problems in timing closure.

The aim of this work is facilitating crossbenchmarking of EMI features for GALS and synchronous design style. It is important to make such EMI analysis, which would let system designers choose optimal solutions to their needs. A first step to make this is to create software able to model and evaluate EMI in synchronous and GALS systems. In this report, we would like to present a software tool able to simulate the EMI behavior caused by clock activity in GALS and synchronous systems on a very high abstract level. This tool is able to model additional features, such as introduced jitter, and phase shifting that can be embedded into GALS or synchronous systems in order to reduce EMI characteristic.

This tool enables performing many simulations in order to investigate the best way to reduce EMI in GALS and synchronous circuits. Several GALS topologies have been evaluated and compared to their synchronous counterparts.
2 REFERENCES

2.1 ACRONYMS

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<tr>
<td>EMI</td>
<td>Electro-Magnetic Interference</td>
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<tr>
<td>GALS</td>
<td>Globally Asynchronous Locally Synchronous</td>
</tr>
<tr>
<td>IP</td>
<td>Intellectual Property</td>
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<tr>
<td>NoC</td>
<td>Network on Chip</td>
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2.2 REFERENCE DOCUMENTS

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3 EMI IN DIGITAL CIRCUITS

3.1 SOURCE OF EMI IN DIGITAL SYSTEMS

EMI in digital systems is caused by the simultaneous switching of logic components. Each active edge of a clock pulse, in a synchronous system, triggers all flip-flops that generate noise. This triggering is not exactly at the same moment because of the clock tree and its skew that spreads triggering of the flip-flops in time. EMI generated by the digital circuits can be analyzed in the easiest way by evaluating the source current shape. Reduction of EMI is possible in several ways including improvement of physical elements. However, we have focused here only on a modification of a clock behavior by adding jitter or a fixed phase to each sub block.

In order to build an exact model of any digital system, we need an accurate current shape profile. It is very difficult to define the current shape for each digital block and in each clock cycle, when the system is defined on a very abstract HDL level. The current profile varies significantly in each design. Moreover, it can change from cycle to cycle depending on activity and processing load. An important issue is to model the current profile in a particular clock cycle. In [BL04] it is shown that for digital systems triangular modeling of the current shape can be used. In Figure 1 triangular supply current is presented both in time-domain and frequency-domain, as given in [BL04]. Value \( I_p \) is a current peak, \( t_r \) is a rise time, \( t_f \) is a fall time. However, different clock cycles may have totally different current shapes depending on the logic activation in the digital block. In principle, the triangular model cannot always satisfy the real behavior of the system. For some complicated cases, we could model the current profile as a superposition of several triangular shapes.

![Figure 1: Triangular approximation of the supply current in (a) time-domain (b) frequency domain](image)

In order to confirm this we have modeled realistic digital synchronous circuits consisting of complex sequential stage (512 flip-flops), combinational logic (813 basic combinational cells), reset and clock tree (369 buffers). We have modeled such system in 0.25 um CMOS technology from IHP and simulated it in different scenarios in Cadence Spectre. Some results are shown in Fig.2. The current shape from 2a) can be modeled with the triangular shape but for 2b) a more appropriate model would be the superposition of two triangles.
3.2 Reducing EMI in Digital Systems

Two techniques are mainly applicable to reduce EMI in synchronous systems by modifying clock behavior [GR05]. First we can add a clock phase shift to each LS block. Phase shift decreases the current peaks for a whole circuit, thus reducing EMI.

Additionally, we can add jitter to the clock source. Jitter introduces a phase modulation (rapid phase fluctuations) to a clock wave from cycle to cycle influencing EMR (Electromagnetic Radiation) [BA04]. It modifies slightly, up to a defined part of a period, the starting point of a rising edge, while the time of the high level stays constant. Hence, jitter can increase or decrease the clock period for a cycle but generally the average base frequency remains the same.

In Figure 3 we gave a summary of methods that can be applied for EMI reduction regardless of the design style (GALS or synchronous). GALS systems are considered as a system of sub blocks that can operate with different frequencies. Thus, applying a phase shift to a GALS sub block would have no impact on EMI reduction, since phase shifting is in nature of GALS systems. For that reason, GALS chips are divided into the traditional ones and low-EMI GALS with jitter applied. On the other hand, the synchronous systems can be divided into the traditional ones and low-EMI. A traditional synchronous system represents a circuit with one clock domain. In order to lower EMI in synchronous systems three add-ons are possible:

- Jitter
- Phase shift
- Jitter + phase shift
Figure 3: Reducing EMI for synchronous and GALS systems

3.3 JITTER GENERATOR

Generally, jitter consists of Pseudo Noise Generator (PNG) and Delay Element (DE), as shown in Fig. 4. Pseudo noise generator is responsible for selecting random delay. The delays are created by a Delay Element that consists in propagating variably delayed signal. However, triggering a Pseudo Noise Generator by an output clock of jitter generator is hazardous. The glitches can occur between two different cycles due to the lack of proper setup time of the Pseudo Noise Generator. A better way to handle this depends on adding an extra delay to the Delay Element. That delay would last longer than a maximal possible jitter size. Thus, the Pseudo Noise Generator would have enough time to set properly its outputs before the next cycle of the clock input occurs. This approach is presented in details in Figure 7.

Figure 4: Structure of the jitter generator
Table 1: First 19 polynomials of LFSRs

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<th>Bits $n$</th>
<th>Feedback polynomial</th>
<th>Period $2^n - 1$</th>
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<tr>
<td>4</td>
<td>$x^4 + x^3 + 1$</td>
<td>15</td>
</tr>
<tr>
<td>5</td>
<td>$x^5 + x^3 + 1$</td>
<td>31</td>
</tr>
<tr>
<td>6</td>
<td>$x^6 + x^2 + 1$</td>
<td>63</td>
</tr>
<tr>
<td>7</td>
<td>$x^7 + x^6 + 1$</td>
<td>127</td>
</tr>
<tr>
<td>8</td>
<td>$x^8 + x^6 + x^5 + x^4 + 1$</td>
<td>255</td>
</tr>
<tr>
<td>9</td>
<td>$x^9 + x^5 + 1$</td>
<td>511</td>
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<td>10</td>
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<td>1023</td>
</tr>
<tr>
<td>11</td>
<td>$x^{11} + x^9 + 1$</td>
<td>2047</td>
</tr>
<tr>
<td>12</td>
<td>$x^{12} + x^{11} + x^{10} + x^4 + 1$</td>
<td>4095</td>
</tr>
<tr>
<td>13</td>
<td>$x^{13} + x^{12} + x^{11} + x^8 + 1$</td>
<td>8191</td>
</tr>
<tr>
<td>14</td>
<td>$x^{14} + x^{13} + x^{12} + x^2 + 1$</td>
<td>16383</td>
</tr>
<tr>
<td>15</td>
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<td>19</td>
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<td>524287</td>
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To build a digital jitter generator, a Linear Feedback Shift Registers (LFSR) can be utilized as a Pseudo Noise Generator (PNG) [GR05]. In GALS systems with a pausable clock, we can only add jitter to a system. Integrating a phase shift would be a useless procedure. Variable phase shift is already present there by the nature of the GALS methodology. Linear Feedback Shift Register is a shift register that generates pseudo-random sequences. LFSR structure is based on polynomials (some of them are given in Table 1). It generates a new input bit by applying a linear function to some of the previous states called taps. There are only two linear functions: xor and inverse-xor. In LFSR the former one is commonly used. The initial state of LFSR is called seed. Seed is a sequence of bits in registers after a reset of a system. Because LFSR is deterministic, it is possible to determine the next and the previous state from the current set of bits. Therefore, it is recommended to use different seeds for jitter generators in order to avoid the same jitter behavior for each block. Moreover, the seed with all 0s is forbidden because LFSR would be permanently in idle state. It is possible to create both hardware and software versions of the LFSR.

The period of the LFSR depends on the number of bits it contains. It can be determined from the equation: $2^n - 1$, where $n$ is a length of LFSR. LFSR feedback can depend on two or more taps as it is presented in table 2.1. There are two types of LFSR:
• Fibonacci LFSR – a new input bit is created by at least two taps. Signals from that taps are XORed and the value is placed in front of the shifter (Figure 5). The last bit is pushed out and all other bits are shifted to the right.

![Figure 5: 16-bit Fibonacci LFSR. The feedback tap numbers correspond to a primitive polynomial in table 1. Hence, the register’s maximum period equals to 65535 states excluding the all-zeroes state which is forbidden.](image)

• Galois LFSR – In contrast to a Fibonacci LFSR, in Galois LFSRs the taps are XORed with the output bit before they are placed in the next register (Figure 6). In particular, when an output bit is equal to “0”, then all taps preserve their values. The register is only shifted to the right and the output bit “0” becomes a new input bit. On the other hand, when the output bit is “1”, then all taps change their value and the register is shifted to the right. The new input bit is “1”. Galois LFSR does not calculate each tap in order to produce a new input bit. Thus, it is faster and calculations can be processed in parallel reducing the propagation time.

![Figure 6: 16-bit Galois LFSR. The register numbers correspond to the same primitive polynomial as the Fibonacci instance in Figure 2.10 but are presented in reverse to the shifting direction. Here also the register’s maximum period equals to 65535 states excluding the all-zeroes state which is forbidden.](image)

The Galois LFSR is commonly used in digital circuits. However, for conducting research and simulations it does not matter which solution is chosen.
In order to create a programmable Delay Element (DE) a chain of invertors or buffers can be utilized. The whole solution for a reasonable jitter generator is presented in Figure 7. It consists of:

- Clock generator (input clock signal)
- Chain of delay elements (each contains two invertors)
- Multiplexer
- 4 bit LFSR

The aim of multiplexer is to select an appropriate delay line that will be propagated to the output (CLKOUT). The LFSR is triggered by the last additionally delayed clock signal (CLKDLY) to avoid any metastability and glitches that could occur at the output of jitter.
An outlook of a behavioral simulation of the jitter generator described before is presented in Figure 8. Clk_max (corresponding to CLKDLY signal in Figure 7) is a signal that triggers the LFSR. It is the maximally delayed signal in order to prevent glitches occurring. Moreover, the LFSR is triggered when all the clock signal (input and output) are in the low state. Thus, there is enough time for registers to complete proper setup. The Sel signal represents a value of LFSR. Although it contains 4 bits, only 3 are used (the coded signal) in order to select 1 out of 8 delay lines that is propagated to the output. It can be clearly observed, that during each cycle, the delay of output clock is propagated according to the selected delay element.

<table>
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<tr>
<th>delay_line</th>
<th>width of high_state (ps)</th>
<th>delayed (ps)</th>
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<tr>
<td>MIN</td>
<td>5178</td>
<td>207</td>
</tr>
<tr>
<td>00000001</td>
<td>5100</td>
<td>357</td>
</tr>
<tr>
<td>00000100</td>
<td>5131</td>
<td>479</td>
</tr>
<tr>
<td>00010000</td>
<td>5071</td>
<td>635</td>
</tr>
<tr>
<td>01000000</td>
<td>5043</td>
<td>906</td>
</tr>
<tr>
<td>MAX</td>
<td>5011</td>
<td>1175</td>
</tr>
</tbody>
</table>

Table 2: Properties of jitter generator

The proposed jitter generator is synthesized using IHP 0.13 um CMOS library and successfully simulated. In the table above (Table 2) there are presented results of simulations of the pseudo random jitter generator at the netlist level. The input clock was 100 MHz (10 ns cycle). "Delay_line" describes which delay is selected. Next, all properties of every delay element are presented. "Width of high_state" describes how long the logic ‘1’ in the output signal lasts. It can be observed that the values are not equal. Comparing to the input clock, which high-state last exactly 5 ns, the output clock’s high-state is a little bit extended. The extension varies from 11 ps up to 178 ps. In the third column, the delay between input clock and output clock transition from logic ‘0’ to logic ‘1’ is presented. Although the delay increases when higher delay element is selected, the increment is not linear. A distinction between two adjacent delay line outputs is not constant. We can assume that the average difference equals to 130 ps and is equal to the propagation time of two combined inverters.

With 100 MHz input clock and 8 delay elements in the delay line, the maximal reduction of an input clock is 10 %. However, replacing delay line with only 4 delay elements would let us to use 200 MHZ input clock with the same maximal reduction of the input clock (10%). There is also a possibility to replace current delay elements (2 combined inverters) with dedicated delay elements. But their propagation time should be shorter than the solution with inverters. In this way would be possible to improve a resolution of a jitter.

### 3.4 Modeling EMI in Digital Systems

In order to evaluate EMI features of the digital systems caused by the digital clock behaviour, we have generated a special software tool called "GalsEmilator". GalsEmilator is a program created in Matlab in order to investigate EMI in various types and topologies of GALS systems (including synchronous solutions). It contains many options to model, as precisely as possible, the parameters of each GALS/synchronous system. Hence, we are able to observe the noise behavior in frequency and time domain. The GUI of this software is given in Fig. 9.
Figure 9: GalsEmilator – software to model EMI in synchronous and GALS systems

In the developed tool, we were trying to enable modelling different current shapes for different clock cycles. In software it is possible to describe up to five different current profiles and specify the probability of their appearance in the system. For each block of the synchronous system, we can also set: a clock phase shift (in respect to the global clock frequency) and additional jitter. For GALS modules, we can model extra clock jitter and also model pausable clocking [MUT00] as a dominant technique for low-EMI GALS circuits.

Simulator description

Figure 10 presents an UML activity diagram for GalsEmilator. It shows the way in which the software should be handled properly. All actions to run a successful simulation are presented step by step.

First of all, it is possible to select, in the simulator GUI, a chip type. There are two previously described designs: GALS or Synchronous approach. In particular, after selecting a synchronous system it is impossible to select several options that are intended for GALS system e.g. “pausable clock”. Moreover, in GALS system, each sub block’s frequency have to be specified, whereas in synchronous system only one is necessary.

Up to five current profiles can be described in the GUI by specifying their shapes in percents. Hence, every current shape will be recalculated according to block’s frequency and sampling frequency creating a matrix of values for every block. Moreover, it is necessary to specify current shape occurrence probability for each of blocks. The values determine how many times per 100 cycles every shape is going to occur. Usually, the equally distributed numbers are placed because, for general tests, it is difficult to define real figures. Next, current waves for sub blocks are calculated in a time domain according to the blocks’ frequencies, current profiles and their probability. Hence, the current waves are composed with a number of single patterns.
At that moment there is possible to define one wave per block. Each wave can be additionally modified according to the features that are described later. Further, all waves are summed into one final wave of a whole chip. The FFT (Fast Fourier Transform) is used in order to move the final wave from the time domain into the frequency domain. After the transformation, it is possible to observe the whole spectrum and the EMI reduction in several ranges of frequency:

- 0 – 0.2 GHz (without 0)
- 0.2 – 0.4 GHz
- 0.4 – 0.6 GHz
- 0.6 – 0.8 GHz
- 0.8 – 1.0 GHz
- 1.0 – 1.2 GHz
- 1.2 – 1.6 GHz
- 1.6 – 2.0 GHz
- 2.0 – 3.0 GHz
- 3.0 – 4.0 GHz
- 4.0 – 5.0 GHz

The ranges of spectrum in the lower frequencies are shorter because the values change more rapidly. On the other hand, in the higher frequencies the spectrum is more flat. Thus, the ranges can be relatively wider. The values of a spectrum are presented in dB regarding the total current supply indicated as current peaks per each sub block.

The second set of options that influences the look of a waveform for each sub block is “Features”. It is possible to set:

- clock phase shift of each sub block (useful only with a synchronous design)
- jitter
- pausable clock (possible only for GALS systems)
- sampling multiplier
- signal length

Clock phase shift option contains additional text input box, where each shift of a block is defined in percents. This feature moves a wave in time according to an indicated fraction (percents) of its period. It can be useful when a mesochronous system is investigated regarding EMI.

Jitter introduces a phase modulation (rapid phase fluctuations) to a waveform. It modifies slightly, up to the defined part of a period, the starting point of a rising edge, while the time of high level stays constant. Hence, jitter can increase or decrease frequency for one cycle but generally the base frequency remains unchanged. With the simulator GUI it is possible to select between random jitter, that uses the Matlab embedded random number generators (with the period of \(2^{9937}-1\)/2) and LFSR (Linear Feedback Shift Register). Selecting the LFSR method is necessary to specify also the LFSR length and the resolution of delay chain. The LFSR length determines a number of bits used to create LFSR, thus the length of the period of a jitter is defined. The resolution of delay chain describes how many possible states of jitter will be applicable for an input clock signal.

Pausable clock option allows simulating GALS wrappers that can stop a clock in order to confirm the handshake operation. It is necessary to specify occurrence probability of a pause and a max delay (fraction of a cycle). The delay length can vary in each step because it is randomized. The length, that is specified, indicates only the worst case.

The two last options are focused indirectly on the whole final wave. Sampling multiplier describes how many times faster would be the sampling frequency in comparison with the highest
frequency of the blocks. It is suggested to remember that the lowest possible sampling frequency is twice the highest measured waves’ frequency (the Nyquist–Shannon sampling theorem). However, usage of the lowest sampling frequency is not recommended because each cycle of the fastest sub block would be modelled only with 2 points. The suggested sampling multiplier is 200, although 100 would be also enough. The latter one is sufficient because a current shape of the fastest module will be modelled with 100 points that is usually enough to present every detail. However, the higher sampling multiplier the more adequate model but also the longer time of computations. The difference in results between that two sampling multipliers was insignificant but not every case has been investigated. Moreover, we can set the signal length. The signal length describes how long will be modelled signal in points.

It should be noticed that each point of a waveform is calculated according to the sampling frequency. Generally, if there would appear a significant difference between two simulations, the signal length should be extended. It ought to reduce the variations between simulations with the same settings caused by several random values e.g. pausable clock or jitter generated by the Matlab random method. If the sampling frequency is too low, it might be also necessary to increase its value in order to improve results.

At the bottom of the GUI two small graphs are present. Although they are embedded into a GUI, there are extra options (checkboxes) that allow user creating the separate flexible charts. Then, all parameters of a chart can be modified. The latter graph shows a current wave in the time domain. The former displays the same wave in a frequency domain after Fast Fourier Transform. The values presented in the chart are compared with the sum of current peaks and presented in dB. Additionally, it is possible to specify the range of frequencies that will be displayed in a chart in order to investigate a fixed area. It facilitates the signals comparing and further evaluation.
Figure 10: UML model of GalsEmulator
3.5 GALS and Synchronous System Modelled in GALS Emulator

Our model of GALS with pausable clocking allows us to simulate GALS wrappers that can pause the clock in order to perform a handshake operation. The behavior can be modeled by setting a probability of pause occurrence and a maximum delay of the pause. The delay is variable and, therefore, in our model it is randomized.

All simulated results, as shown in Fig. 9, can be observed and analyzed both graphically and in a generated table. The complete software has its own user-friendly GUI.

We have utilized our software to model and evaluate EMI of different GALS and synchronous systems. For the GALS approach, we have concentrated on the pausable clocking scheme, that is very commonly used even in today’s GALS NoC systems [MUT00, BEI08]. In order to exactly model the clock behavior of the GALS system, all evaluated systems have been described in VHDL and simulated. The clock behavior is automatically extracted from the simulation using our software tool. Data is directly fed to the EMI analyzer and evaluated. Such extension of our tool was necessary in order to achieve one-to-one matching to the real system behavior of the GALS interfaces. Especially, it was difficult to extract, without real simulation data, clock behavior during the data transfer process between the GALS blocks when clocks can be paused.

Figure 11: Sample of connection between two adjacent LS blocks used in models

In our VHDL models, we have used D-type output and P-type input GALS ports [MUT00] as shown in a Figure 11. ‘Demand Type’ (D-type) ports pause the clock immediately after receiving request from the Locally Synchronous (LS) block. For the input side, ‘Poll Type’ (P-type) ports have been used. The standard handshake operation between adjacent GALS modules was completely modeled in our simulation. The behavior of the clocking changes dramatically with the intensity of the data transfer since the clock pausing appears only during the data transfer process. Therefore, we have modeled three different scenarios of the system behavior:

A. Low data transfer, where the data transfer is performed relatively rarely (once per 6 clocks in the example we were using)
B. Medium-to-high data transfer, where half of the clock cycles are involved in data transfer
C. Burst mode, where more than 80% of the clock cycles are data transfer related.

Topologies of the evaluated GALS systems: In our evaluation four different structures of GALS circuits have been analyzed as shown in Figure 12. We have analyzed different system topologies. Here, we have taken into consideration point-to-point (a), star (b) and mesh (c) topologies. In order to check if a granulation can influence the reduction of EMI, we have also examined the star with a large number of blocks (d). The goal was to evaluate different interconnect structures and to see their impact on EMI in GALS systems. The arrow in the Fig. 12 indicates a direction of handshake and data transfer.
System parameters of the model: For the system modelling, we have defined a base frequency which is a median for all other derived clock frequencies in the system. We needed such a frequency to be able to compare a synchronous system that normally has just a single clock domain with a GALS system that is usually triggered with different clocks. In our model this base frequency was 50 MHz. GALS systems can be implemented very differently. Some systems may use very similar clock frequencies for local blocks (plesiochronous clocking). On the other hand other systems may have totally different LS clock frequencies. Generally, we used 3 different frequency sets for modules in our GALS systems. The first set represents plesiochronous operation where the frequencies of each block are almost the same as the base frequency. In the second set, the difference is higher and in the third one, we have frequencies ranging up to a ratio of 1:3.

It can also make a difference which block has the slowest and which block the highest frequency. In particular, for the star topology, if the slowest block is in the centre, the complete system will be very slow and vice versa. We have tested, therefore, the star topology with both slow and fast setting.

In all cases, we have used 10 GHz sampling frequency. This sampling is quite sufficient for the systems we were modelling since the current profile with 50 MHz clock was represented as 200 points in simulation. In the model, we have used equal probability of occurrence for each of the five modelled current shapes. Also, we have used the same jitter settings for each simulation, with the LFSR length of 15 bits. The sum of the current peaks in all cases was the same in order to correctly compare results. In the 4-module systems we have defined that the peaks were 100 mA, 400 mA, 200 mA, and 300 mA. In 10-module systems the distribution was following: 2 X 200 mA, 4 X 100 mA, 4 X 50 mA.

### 3.6 Comparing Synchronous and GALS Systems

**Synchronous system:** In Figure 13, we can observe the EMI characteristic and its reduction in synchronous systems. In particular, we can see the EMI reduction in the synchronous system with a jitter applied. As we can notice, the jitter reduces only higher frequencies starting from 400 MHz. It has no significant influence to the lower spectral range. However, to achieve the reduction, the circuit should be able to be immune to 10% jitter, what is not so easy in a synchronous design, both for hold and setup time optimization. Moreover, Fig. 13 shows the effect of adding a phase shift to a system. We have modelled case with 10 different synchronous sub-blocks with optimized phase shift. By introducing a phase shift to a circuit, we can alleviate EMI in a low frequency range, thus reducing current peaks. The high frequency spectrum remains not significantly changed compared to a basic synchronous approach. The tests were conducted also with a combination of jitter and phase shift. The results are very promising because they incorporate advantages of both features. However, it would be a real challenge to guarantee safe data transfer between blocks in such synchronous system.
Figure 13: EMI characteristic in the synchronous systems

In Figures 14 and 15 the single-sided amplitude spectrums are presented. The former figure presents a spectrum of a totally synchronous 10-module design. The latter one presents the same system with the phase shift and the jitter feature applied. A significant lowering of envelope can be observed. Moreover, the peaks in a system with phase shift and jitter are almost totally prevented. There are only few in a low range of frequencies. In order to alleviate them, it would be necessary to reduce current peaks in a system, which is not a trivial task.

Figure 14: Power spectrum of supply current for the pure synchronous circuit
Figure 15: Power spectrum of supply current for the 10-module synchronous circuit with added jitter and phase shifts distributed: 0%, 50%, 20%, 40%, 70%, 90%, 10%, 30%, 60%, and 80%

Evaluating GALS systems: Figure 16 represents results of comparing two sets of frequencies with medium data transfer and also showing the behaviour for low granularity systems (4 GALS blocks) and high granularity systems (10 GALS blocks). We can observe that plesiochronous systems can achieve a significant EMI reduction in the high frequency range. However, it doesn’t improve EMI for low frequency operation. On the other hand, the GALS system, with a larger difference of frequencies, reduces much better EMI of low frequencies in a spectrum, still preserving good parameters for higher frequencies. The test performed on various transfers rate with the same frequencies has shown very low differences in EMI reduction. The range of the result variations didn’t exceed 5 dB.

Figure 16: EMI characteristic in GALS systems with different frequencies set and jitter
Figure 16 shows the EMI reduction in GALS systems with added jitter. We can observe that there is almost no impact of jitter at low frequencies. It remains almost the same as in GALS systems without jitter. However, the higher frequency range is more attenuated giving a better reduction of EMI. Every set of frequencies has a similar spectrum starting from 400 MHz and we can observe reductions around 15 dB.

Comparing different topologies of 4-modules GALS systems: point-to-point, mesh and star, we have noticed a similar behaviour. There is a very little influence of data rate transfer intensity on EMI reduction. The most important parameter is the frequency of LS blocks. The more frequency spread, the better EMI reduction in the lower spectrum. Moreover, in each case jitter has a positive effect on reduction of EMI. It significantly reduces higher frequencies in a spectrum. The average reduction of EMI for all 4-module topologies in comparison to a totally synchronous system is around 20 dB starting from 400 MHz.

We can extract similar results from a star topology with more satellite blocks. However, we notice a greater difference in EMI reduction after adding jitter. The worst results are observable with the frequencies set, where the center block is the slowest one. The best results, in respect to EMI, are achieved when the center block is the fastest one. Hence, we can conclude that the most reasonable architecture from the point of view of the performance, with the fastest center block, is also the most appropriate approach for EMI reduction.

We have also compared the effect of block granularity to the final results. Comparing 4-module and 10-module GALS system, we can observe the better results for the more granular design. In Figure 16 this can be clearly observed. The gain reduction is around 5 dB. In general, it means that the finer the granularity of the system the better reduction of EMI.

Figure 17: Comparing the results from Synchronous and GALS systems

In Figure 17 combinations of both systems are presented. We have selected a standard synchronous system, synchronous system with phase shift and jitter, and a GALS system with high block granularity and with jitter. We can notice that the results of the low-EMI synchronous system are around 5 dB worse than the GALS system with the best EMI characteristic. In the low-EMI GALS system EMI is reduced around 25 dB compared to the classical synchronous approach.

If we use absolutely best results from synchronous approach (perfect matching of the clock phases of each sub-block, avoiding any overlap) the comparison results between low-EMI GALS and low-EMI synchronous became very similar with very slight differences. This is shown in Fig. 18. However, such synchronous system would be difficult to be implement and it will cause very big design effort to plan and implement such careful clocking of the system with correct timing closure.
3.7 CONCLUSIONS

In this section, the GALS methodology was investigated in order to evaluate the ability for EMI reduction. We have generated a software tool based on Matlab to simulate EMI properties of the digital GALS systems. It supports simulations of GALS/synchronous systems with different granularity, frequencies, current shapes, topology, and other parameters. Using the software, we have modelled different GALS and synchronous systems in order to evaluate different topologies, architectures and EMI reduction techniques.

The results show that the reduction of high spectral components can be successfully achieved with jitter introduction. EMI at low frequencies can be reduced by a phase shift introduction for synchronous systems. However combining those two features would be hard in synchronous systems because of data transfer between blocks. In GALS systems, phase shift is already present by the nature of the GALS methodology. Local clock generators also naturally generate clocks with jitter, but this feature of ring oscillators was not deeply analyzed here. In this work, we have modelled explicit jitter introduction with the special jitter generators based on LFSR structures. By adding jitter in a GALS system, we can achieve a significant reduction over whole spectrum, not affecting the functionality of a system. The reduction of over 20 dB can be achievable, as illustrated in the results. Moreover, the current peaks in time domain can be reduced up to 40% in GALS systems. We have found that there is almost no correlation between EMI reduction and data transfer intensity (i.e. clock pausing rate) in GALS modules. The greatest impact has the used set of frequencies and the granularity of GALS partitioning.

Finally, comparing low-EMI synchronous solutions and GALS methods, we can conclude that low-EMI GALS approaches give better results than synchronous approaches and similar to low-EMI synchronous approaches.

Figure 18: Comparing the best results from Synchronous and GALS systems
If we compare the differences in time domain for the classical synchronous and the low-EMI GALS system (10 blocks, star topology with jitter), we can observe 40% current peak reduction.
4 GALS FFT DESIGN FOR EMI REDUCTION

4.1 FFT Structure

The block diagram of the pipelined 64-point GALS FFT processor is shown in Fig. 19. To minimize the hardware complexity, the 64-point FFT is divided and conquered by two cascaded 8-point FFT computation. For each 8-point FFT, the novel Radix-23 FFT algorithm is developed and utilized, which has 3 stages of the butterfly (BF) structure. Based on this architecture, only one complex twiddle factor multiplier is required to perform pipelined 64-point FFT.

Figure 19: GALS FFT Processor

4.2 FFT Algorithm and Architecture

To reduce the electromagnetic interference (EMI) of the digital circuits, in particularly the power and ground bounce caused by the simultaneous switching noise (SSN), which is critical for analog/digital mixed circuits design, the pausible clocking based GALS design is implemented as shown in Fig. 19. Each synchronous block is surrounded by an asynchronous wrapper, which consists of a local clock generator and a number of asynchronous I/O ports. By exploring the clock modulation on each block, significantly reduction in the sharp peaks of the system supply current, and consequently the bounce on the power and ground rings, can be expected.

4.2.1 System Partition

There are totally seven functional sub-modules in the pipelined 64-point FFT processor, including six butterfly structures and one complex multiplier. To reduce the peaks on supply current, these sub-modules have been grouped and partitioned into four synchronous blocks according to the power and current consumption. To estimate the power consumption accurately, the dynamic power analysis is performed based on the simulation waveforms of the synthesized netlist using the IHP 0.13µm CMOS standard cells library. Tab. 3 presents the partition scheme of the GALS FFT processor, where each block has the similar contribution to the system power and current consumption.
4.2.2 Clock Modulation

Two techniques of the clock modulation, phase modulation and frequency modulation, have been applied to the pausible local clock signals of four synchronous blocks.

Phase Modulation

For each pausible clock generator, its output clock is first propagated through a programmable delay line. By programming the delay line, the rising edge of each clock can be shifted independently. These clock shifting results in the spread on the switching activities of the synchronous blocks, and therefore, the sharp peaks on the system supply current will be reduced substantially. In the experiment, the clock signals of four synchronous blocks are shifted and evenly allocated within the clock period, as shown in Tab. 4. For instance, the evenly distribution of supply currents of four synchronous blocks is clearly illustrated in Fig. 20.

<table>
<thead>
<tr>
<th></th>
<th>Sync. Block 1</th>
<th>Sync. Block 2</th>
<th>Sync. Block 3</th>
<th>Sync. Block 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Function</td>
<td>BF Stage 1</td>
<td>BF Stage 2/3</td>
<td>Complex Mult.</td>
<td>BF Stage 4/5/6</td>
</tr>
<tr>
<td>Area (µm²)</td>
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<td>46119</td>
<td>47459</td>
<td>40547</td>
</tr>
<tr>
<td>Number of FF</td>
<td>651</td>
<td>637</td>
<td>173</td>
<td>362</td>
</tr>
<tr>
<td>Average power (mW)</td>
<td>1.2</td>
<td>1.5</td>
<td>1.2</td>
<td>1.7</td>
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<tr>
<td>Average current (mA)</td>
<td>1</td>
<td>1.25</td>
<td>1</td>
<td>1.4</td>
</tr>
</tbody>
</table>

Note: (1) Reported by Synopsys DesignCompiler;
(2) Reported by Synopsys PrimeTime at 80MHz working frequency.

4.2.2 Clock Modulation

Two techniques of the clock modulation, phase modulation and frequency modulation, have been applied to the pausible local clock signals of four synchronous blocks.

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<table>
<thead>
<tr>
<th>t_CLK⁻⁺</th>
<th>Sync. Block 1</th>
<th>Sync. Block 2</th>
<th>Sync. Block 3</th>
<th>Sync. Block 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>T_CLK/4</td>
<td>T_CLK/2</td>
<td>3T_CLK/4</td>
<td></td>
</tr>
</tbody>
</table>

Figure 20: Current Profile of four synchronous blocks

Phase modulation is also applied on the traditional synchronous design to re-shape the supply current, where the intended clock latency and clock skew are introduced in the global clock tree networks to spread switching activities. However, due to the setup-time and hold-time constraints, the clock phase modulation is restricted in a rather small range (typically less than 5%TCLK). On the contrary, attributed to the asynchronous communication between blocks in the GALS design, there is no constraint on the phase modulation of synchronous blocks (25%TCLK in the experiment for example). It means that phase modulation can be optimized in terms of minimum peaks on current in GALS designs.
**Frequency Modulation**

Another approach to reduce EMI/SSN is to randomize the working frequency of the digital circuits, which spreads the supply current in spectrum. In the experiment, clock jitter is introduced to modulate its frequency. Fig. 21 depicts a jitter generator and the corresponding clock period variation. The output clock from the phase modulator is propagated through a set of delay lines with different length, and a multiplex is employed to select a delay version of the input clock as the output clock. Simply changing the control coding scheme of the multiplex, we can modulate the clock jitter in diverse modes using this structure, such as linear modulation or pseudo-random modulation. However, to achieve different jitter modes, the control coding scheme needs to be designed carefully to avoid any potential glitch on the output clock. The single-hot coding is utilized to modulate the clock in a triangular (linear) mode, in which the clock period $T_{CLK}$ changes from $(T_{CLK}-4\Delta)$ to $(T_{CLK}+4\Delta)$ with a modulating granularity $\Delta=0.15$ns. To further randomize the frequency of the system, four local clocks are initialized with different offsets on $T_{CLK}$.

![Diagram](image)

**Figure 21:** Triangular modulation of clock frequency

### 4.3 Simulation Results

To compare the performance of synchronous FFT and GALS FFT in terms of EMI/SSN, we develop a test model in MATLAB. The information about system partition and clock modulation on each block is used in the model to generate the current profile. Fig. 22 presents a comparison in the spectrum of supply current from 0 to 20GHz in two modes. It can be observed there is an in average more than 10dB attenuation in the frequency domain by utilizing clock modulation based on GALS design with respect to the traditional synchronous design.
The pipelined 64-point FFT processor is fabricated in the IHP 0.13µm-1.2v sixfold-metal standard CMOS technology. The die size is 1730 µm x 1730 µm with 52 IO pads, as shown in Fig. 23. The chip is packaged in a 64-pin PQFP, and the packaged chip is successfully tested and measured in July, 2009.

For this chip we have measured the supply voltage (Vdd) in frequency domain when the chip worked in different modes. The comparison of the Vdd spectrum is shown in Fig. 24, and the corresponding reduction in dB in the spectral peaks is shown in Fig. 25.
Figure 24: Spectrum of the Vdd in I Synchronous mode, II Synchronous mode with clock jitter, III GALS mode, and IV GALS mode with clock jitter
Figure 25: Reduction in the spectral peaks at p-th clock harmonics

(Red line: synchronous mode with clock jitter, Blue line: GALS mode with clock jitter)

What we can observe from the measurement is that even relatively simple GALS system introduces significant EMI reduction (11 dB of the main peak). Additionally, jitter introduction reduces further, especially higher harmonics. What those measurements also show is a great matching between our simulation model and actual chip behaviour. Simulated EMI gain was around 10 dB and measured was 11 dB.
### APPENDIX A - TABULAR RESULTS

**Table A.1** Results of simulations for the 4-module synchronous system with and without jitter, with different sets of phase shift per each module.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Simulation number</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
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</thead>
<tbody>
<tr>
<td>Phase Shift [%] per module</td>
<td>0 - 0,2</td>
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<td>-20,911</td>
<td>-38,326</td>
<td>-26,955</td>
<td>-37,013</td>
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<td>-57,427</td>
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</table>

Simulation Results [dB] at 11 frequency ranges [GHz]
Table A.2 Results of simulations for the 10-module synchronous system without jitter and with different sets of phase shift per each module.

<table>
<thead>
<tr>
<th>Simulation number</th>
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<td>55</td>
<td>70</td>
<td>20</td>
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<td>50</td>
<td>65</td>
<td>90</td>
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<td>Results [dB] at 11 frequency ranges [GHz]</td>
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</tr>
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Table A.3 Results of simulations for the 10-module synchronous system with jitter and different sets of phase shift per each module.

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Table A.4 Simulation results for the 4-module GALS point-to-point topology system without clock jitter, with different sets of frequencies (1, 2, 3) and various data transfer scenarios (A, B, C) described in details in the previous chapter.

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<th>B3</th>
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Jitter

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Table A.5 Simulation results for the 4-module GALS point-to-point topology system with clock jitter, with different sets of frequencies (1, 2, 3) and various data transfer scenarios (A, B, C) described in details in the previous chapter.

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<th>A3</th>
<th>B1</th>
<th>B2</th>
<th>B3</th>
<th>C1</th>
<th>C2</th>
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<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
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<td>-19,42</td>
<td>-27,72</td>
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<td>-102,89</td>
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Table A.6 Simulation results for the 4-module GALS star topology system without clock jitter, with different sets of frequencies (1, 2, 3) and various data transfer scenarios (A, B, C) described in details in the previous chapter.

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Table A.7 Simulation results for the 4-module GALS star topology system with clock jitter, with different sets of frequencies (1, 2, 3) and various data transfer scenarios (A, B, C) described in details in the previous chapter.

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Table A.8 Simulation results for the 10-module GALS star topology system without clock jitter, with different sets of frequencies (1, 2, 3, 4, 5) and various data transfer scenarios (A, B, C) described in details in the previous chapter.

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Table A.9 Simulation results for the 10-module GALS star topology system with clock jitter, with different sets of frequencies (1, 2, 3, 4, 5) and various data transfer scenarios (A, B, C) described in details in the previous chapter.

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Table A.10 Simulation results for the 4-module GALS mesh topology system with and without clock jitter, with different sets of frequencies (1, 2, 3) and various data transfer scenarios (A, B, C) described in details in the previous chapter.

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<th>A3</th>
<th>B1</th>
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